Programmes After Market Services
NHM-2/5nx,ny/6/9 Series Transceivers

System Module

Issue 2 (April 02)

Table of Contents

Page No

List of Figures

This page intentionally left blank

Baseband

The HDa12 Baseband architecture is similar to DCT3 phones. All the ASICs are in the uBGA package. COBBA GJP, which has a serial interface to the MAD, is used. EEPROM is software emulated in the Flash-memory.

The HDa12 phone supports 'ELVI' (DCT3) and 'Jeanette' (DCT4) chargers, both 2-wire and 3-wire, but when using 3-wire chargers, then the 3rd. wire (charger control input) is connected to Ground by the phone.

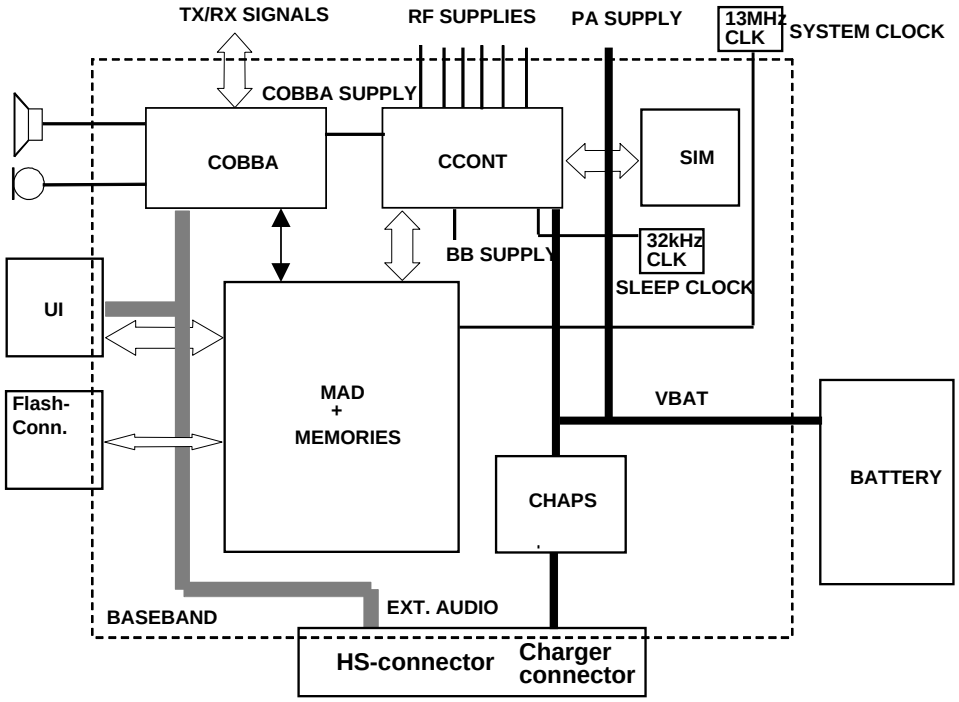


Figure 1: Block Diagram

Technical Summary

The baseband module includes four ASICs: CHAPS, CCONT, COBBA-GJP and MAD2WD1, which take care of the baseband functions of the engine. The baseband is designed to work with the DCT-4 type direct conversion RF.

The baseband is running from a 2.8V power rail (VBB), which is supplied by a power controlling ASIC CCONT. In the CCONT there are 6 individually controlled regulator outputs for RF-section and two outputs for the baseband. In addition, there is one +5V power supply output (V5V). The CCONT contains also a SIM interface, which supports both 3V and 5V SIM-cards. A real time clock function is integrated into the CCONT, which utilizes the same 32kHz clock supply as the sleep clock. The battery charging is controlled by a PWM-signal from the CCONT. The PWM duty cycle is determined by charging software and is fed to the CHAPS charging switch.

The baseband architecture supports a power saving function called "Sleep-mode". In Sleep-mode, the VCTCXO is shut off, which is used as system clock source for both RF and baseband. During the Sleep-mode, the system runs from a 32 kHz crystal. The phone is waken up by a timer running from this 32 kHz clock supply. The sleeping time is determined by some network parameters. The sleep mode is entered when both the MCU and the DSP are in standby mode and the normal VCTCXO clock has been switched off.

The MAD2WD1 is a dual voltage circuit using VBB (2.8V Baseband supply) and VCORE (1. 975V. Core Voltage supply for MAD2WD1 ver. C05).

The interface between the baseband and the RF section is mainly handled by a COBBA ASIC**.** COBBA provides A/D and D/A conversion of the in-phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the user interface. The COBBA supplies the analog TXC and AFC signals to RF section according to the MAD2WD1 DSP digital control. Data transmission between the COBBA and the MAD2WD1 is implemented using serial bus for high speed signaling and for PCM coded audio signals. Digital speech processing is handled by the MAD2WD1 ASIC. COBBA is a dual voltage circuit, the digital parts are running from the baseband supply VBB (2.8V) and the analog parts are running from the analog supply VCOBBA (2.8V).

The baseband supports both internal and external microphone inputs and speaker outputs. Source selection and gain control of the Input and output signals is done by the COBBA according to control messages from the MAD. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD and transmitted to the COBBA for decoding.

An UI-Switch N400 is used as HW-driver for: LEDs, Buzzer and Vibra. Buzzer and Vibra (internal) alert control signals are generated by the MAD2WD1 with separate PWM outputs.

IrDa is not supported by the HDa12.

Flashing of the phone is done in either of two ways:

- By Aftersales using the 4-poled 'Test Flash Connection' pos.: X201 and a 'HDa12 Service battery'.
- In Production using the 8-poled 'Production Flash Connection' pos.: X202.
  (PADs located on the Keyboard side of the PCB).

EMC shielding is implemented using three metal cans: two for the RF and one for the Baseband. Heat generated by the circuitry will be conducted out via the PCB ground planes.

External Signals and Connectors

This section describes the external electrical connection and interface levels on the base-band. The electrical interface specifications are collected into tables that cover a connector or a defined interface.

System/ DC (charger) connector (X200)

DC (charger) connector is physically integrated in the same component as the System-connector (accessory interface). DC connector has both jack and contact pads for desk stand.

An internal 1.5A Fuse in serial with CHRGR+ protects the phone against hazardous Charge current faults e.g. caused by 'Pirates' or defective chargers.

Table 1: System / DC(charger) Connector

Pin	Name	Min	Max	Unit	Notes
1	MIC+				Internal Microphone +see Doc /14/
2	MIC-				Internal Microphone -see Doc /14/
3	CHRGR+	0	16.9	V	Max. open voltage for ACP-7
		0	850	mA	Max. charge-current with ACP-9
4	GND	0	0	V	
5	DC_CRL	0	0	V	Charger Control is grounded.
6	XMICP				External Microphone connector +see Doc /14/
7	XMICN				External Microphone connector -see Doc /14/
8	XEARP				External Earpice connector +see Doc /14/
9	XEARN				External Earpice connector -see Doc /14/
10	INT				Headset detectsee Doc /14/

The Pad- number description in the Figure below shows the lower part of the PCB component-side including pin-numbers of various connectors and Audio components.

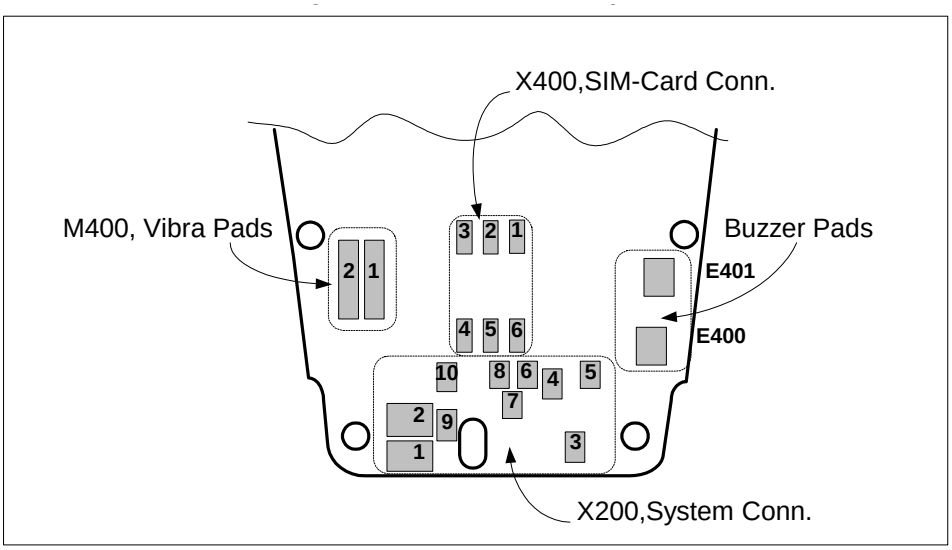


Figure 2: Pad Number description

Test Flash-Connector (X201)

The Test Flash-Connector is used as a flash programming interface for updating (i.e. re-programming) the flash program memory and as an electrical interface for access to the engine by service-tool (e.g. WinTesla). This Interface is typically used by Aftersale via a 'HDa12 Service battery' and by the FINUI- and Label- stations in the factory.
The Connector is made as 4 Test Pads which are accessible through the mechanic of the phone when the Battery is removed.

When the flash programming-tool is connected to the phone (via 'Service battery'), supply power is provided through the battery contacts and the phone is powered up with an IBI-pulse given to the BTEMP line**.**

Note*:ESD protection is applied to all pads of X201*.

Table 2: Test Flash-Connector Electrical Specification

Pin	Name	Parameter	Min	Typ	Max	Unit	Remark
1	FBUS_TX	Data ack. to the Prommer	0 2.24	logic low logic high	0.62 2.85	V	Transmit Data from MAD2WD1 (AccTxData) to Prommer (@ VBB=2,85V)
2	FBUS_RX	Serial data from the Prommer	0 1,68	logic low logic high	0.84 2.85	V	Receive Data from Prommer to MAD2WD1 (AccRxData) (@ VBB=2,85V)
3	GND	GND	0		0	V	Ground
4	MBUS	Serial clock from the Prommer	0 1,68	logic low logic high	0.84 2.85	V	Prommer detection and Serial Clock for synch. Comm. to MAD2WD1 (MBUS) (@ VBB=2,85V)

VPP/ VPP_GND Connector (For Label Station)

To speed up Flash-programming at the Label station in the Production, +12V for VPP and VPP_GND are accessible through the mechanic of the phone, when the battery is removed. The label from the Label-station hides the pads after use.

Table 3: VPP/VPP_GND Connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Remark
J212	VPP	Flash Prog. Volt.	11.4	12.0	12.6	V	Intel Spec. (Worst-case)
J213	VPP_GND		0		0	V	Connect to GND when VPP= +12V

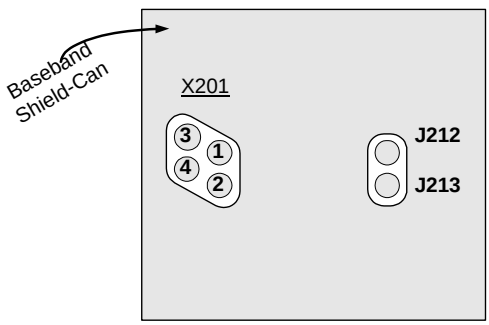


Figure 3: X201 and VPP/VPPGND pad

Production Flash-Connector (X202)

The HDa12 is made in panels of the DCT4 panel-standard. This panel-standard has no space for Production Flash connections, so the Production Flash I/F is placed on the Phone itself.
The Production Flash-Connector includes the same connections as the Test Flash-Connector plus some more as described in table 4.
The Connector is made as eight Test Pads, which are accessible from the Keyboard-side of the PCB, only when the phone is without mechanical covers.

Table 4: Production Flash Connector Electrical Specification

Pin	Name	Parameter	Min	Typ	Max	Unit	Remark
1	CHRGR+	Charger input	0	8.4	12	V	DC input
2	VPP	Flash Programming voltage	11.4	12.0	12.6	V	Intel Spec. (Worst case)
3	MBUS	Serial clock from the Prommer	0 1,68	logic low logic high	0.84 2.85	V	Prommer detection and Serial Clock for synch. Comm. MAD2WD1 (MBUS) (@ VBB=2,85V)
4	GND	Signal Ground	0		0	V	Signal Ground is connected directly to GND.
6	VPP_GND		0		0	V	Connect to GND when +12V is applied to VPP. This is to protect MAD2WD1 VPP output from excessive Voltages.
7	FBUS_TX	Data ack. to the Prommer	0 2.24	logic low logic high	0.62 2.85	V	Transmit Data from MAD2WD1 (AccTxData) to Prommer (@ VBB=2,85V)
8	FBUS_RX	Serial data from the Prommer	0 1,68	logic low logic high	0.84 2.85	V	Receive Data from Prommer to MAD2WD1 (AccRxData) (@ VBB=2,85V)
9	WDDISX	Watchdog disable	0 VBATT–0.7V	logic low logic high	0.5 VBATT	V	Active low

The Figure below shows the lower part of the PCB Keyboard-side with the position and

pin-numbers of X202.

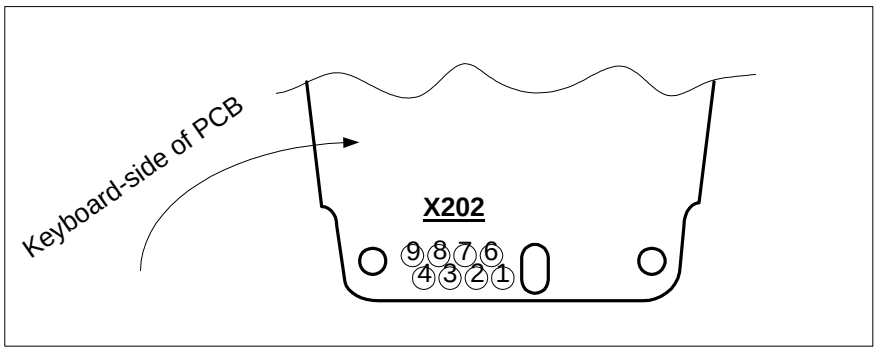


Figure 4: Production Flash Connector

Battery Connector (X203)

The electrical specifications for the battery connector are shown in Table 7. The BSI contact on the battery connector is used to detect when the battery is removed. This is to be able to shut down the operations of the SIM card before the power is lost if the battery is removed with power on.
The BSI contact disconnects earlier than the supply power contacts to give enough time for the SIM shut down.

Table 5: Battery Connector Electrical Specification

Pin	Name	Min	Typ	Max	Unit	Notes
1	VBATT	3.1	3.6	5.2	V	Battery voltage
2	BSI	0		2.85	V	Battery size indication Phone has 150kohm pull up resistor. SIM Card removal detection (Threshold is 2.4V@VBB=2.8V)
		2,2		51	Kohm	"Nickel Battery" Size indication resistor
			22		Kohm	"Service Battery" indication resistor
		56		130	Kohm	"4.2v Lithium Battery" Size indication resistor
3	BTEMP	0		1.4	V	Battery temperature indication Phone has a 100k (+-5%) pullup resistor, Battery package has a NTC pulldown resistor: 47kΩ +-5%@+25C, B=4050+-3%
		2.1 5	10	3 20	V ms	Phone power up by battery (input) Power up pulse width (IBI)
		0		1	Kohm	Local mode initialisation (in production)
4	GND	0		0	V	Battery Ground is connected directly to GND.

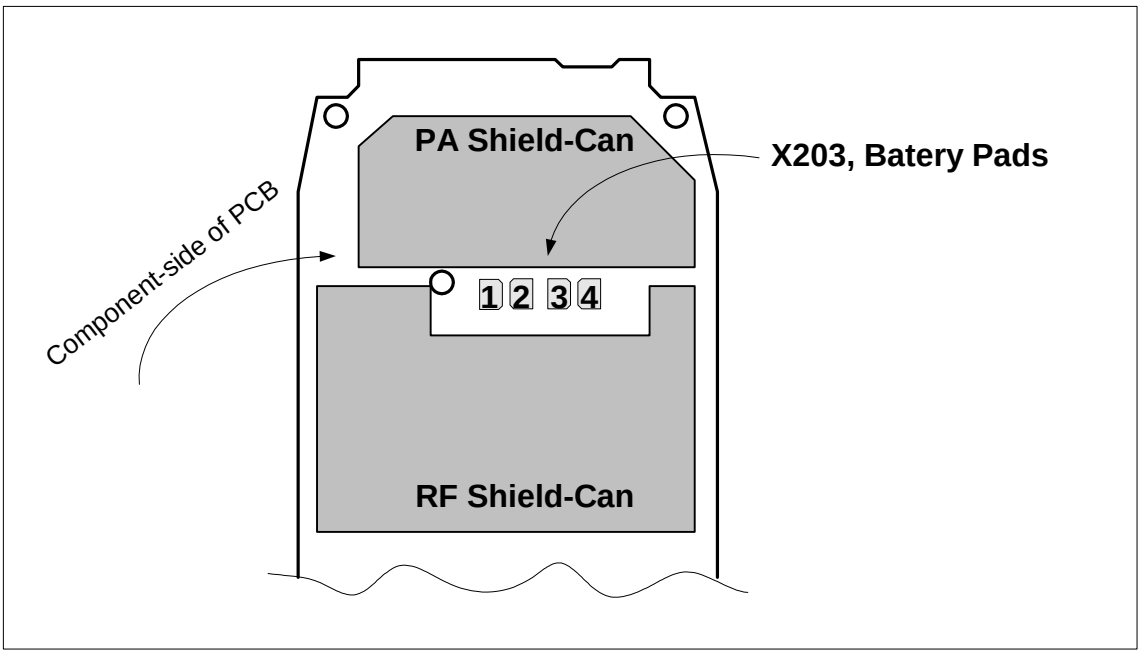


Figure 5: X203 Battery Pads

SIM card connector (X400)

The SIM I/F does not support other voltages than 3V and 5V.
The SIM card connector is located outside the BB-shield can close to the System Connector.

Table 6: SIM Connector Electrical Specification

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
1	SIMCLK	Frequency Trise/Tfall		3.25	 25	MHz ns	SIM clock
2	SIMRST	5V SIM Card 3V SIM Card	4.0 2.8	"1" "1"	VSIM VSIM	V	SIM reset
3	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
4	GND	GND	0		0	V	Ground
5	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
6	DATA	5V Vin/Vout 3V Vin/Vout	4.0 0 2.8 0	"1" "0" "1" "0"	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1us

VSIM supply voltages are specified to meet type approval requirements regardless the tolerances in components.

Internal Signals and connections

LCD Module Interface

Table 7 is a summary of the GD47 LCD Electrical Specification.

Table 7: LCD Module Interface

Pin	Line Symbol	Parameter	Min	Typical / Nominal	Maximum	Unit	Notes
1	VBB	Supply voltage	2.7	2.8	3.3	V	
					240	uA	
2	SCLK	Serial clock input	0		4.0	MHz	
			0		VBB	V	
3	SDA	Serial data input	0 0.7xVBB		0.3xVBB VBB		
4	LCDCDX (ROW5)	Control/display data flag input	0 0.7xVBB		0.3xVBB VBB		Control Data
5	LCDCSX	Chip select input	0 0.7xVBB		0.3xVBB VBB		Active Low
6	GND	Ground		0			
7	VOUT	DC/DC voltage converter output	6	-	9		
8	LCDRSTX	Reset	0 0.7xVBB		0.3xVBB VBB		Active Low

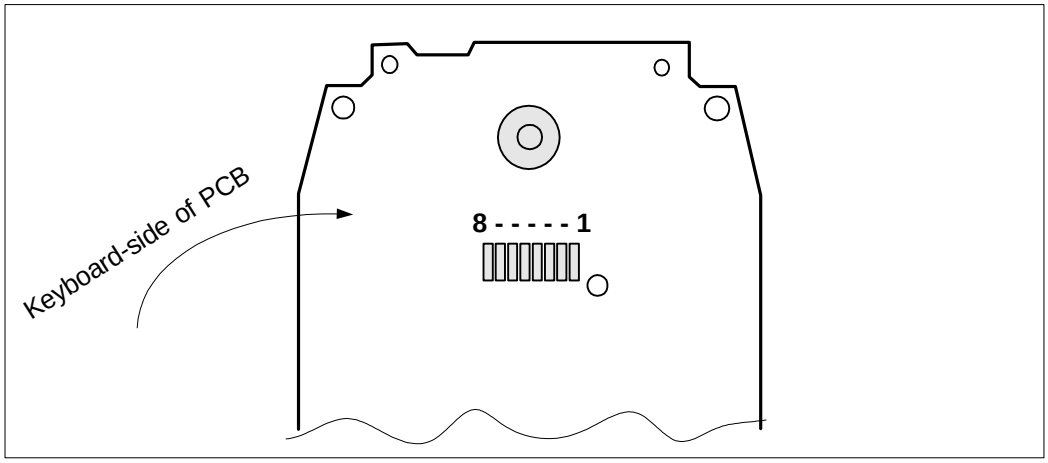


Figure 6: GD47 LCD Pin Numbers

Power Distribution

In normal operation, the baseband is powered from the phone's battery.
An external charger can be used for recharging the battery and supplying power to the phone.

The baseband contains parts that control power distribution to whole phone excluding those parts that use continuous battery supply. The battery feeds power directly to the CCONT and UI (buzzer and LEDs for display/ keyboard). Figure 7, "Baseband Power Distribution," on page 15 shows a block diagram of the power distribution.

The power management circuit CHAPS provides protection against over-voltages, charger failures and pirate chargers etc. that would otherwise cause damage to the phone.

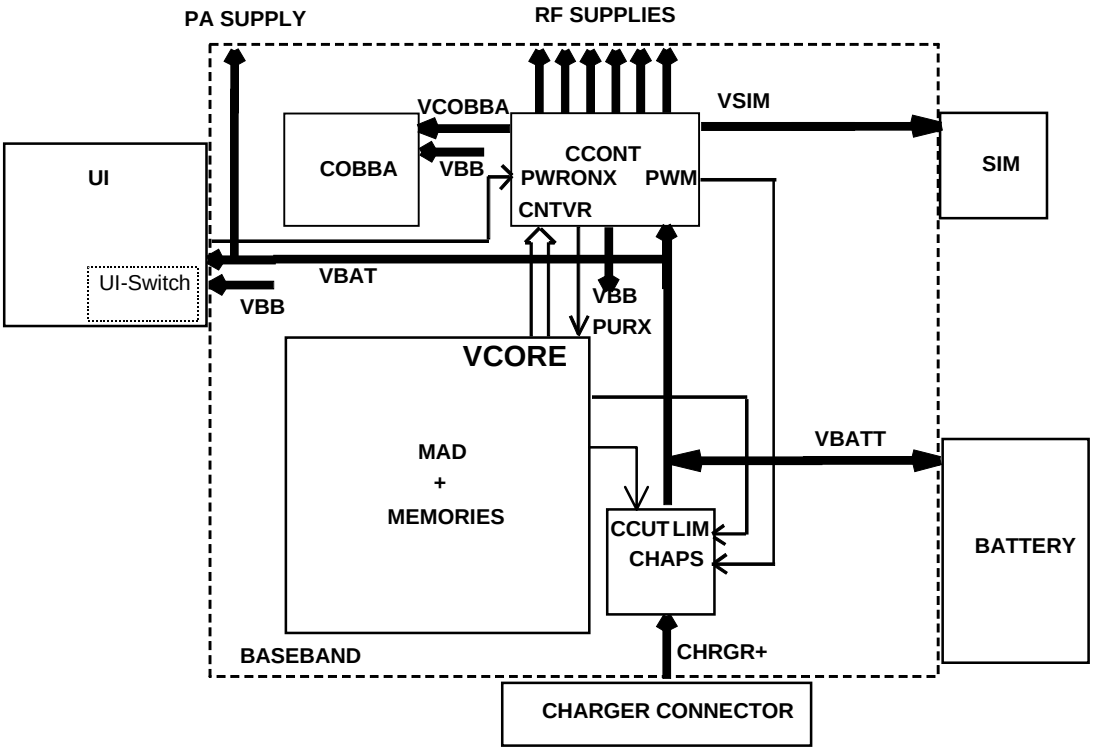


Figure 7: Baseband Power Distribution

Battery Charging

The electrical specification gives the idle voltages produced by the acceptable chargers at the DC connector input (CHRGR+). The absolute maximum input voltage is 30V, due to the transient suppressor that is protecting the charger input. At phone end there is no difference between a plug-in charger and a desktop charger because the DC-jack pins and bottom connector charging pads are connected internally in the System connector. The control-line of three terminal chargers is connected to GND on the PCB.
Charger ground is also connected directly to GND on the PCB.

The purpose of the Capacitor on the CTIM pin is to reduce Output Current slew-rate of the CHAPS. This is to minimize switching noise in the Audio circuits.
The CTIM-pin is also controlled by the MAD-signal CCUT. When CTIM is shorted (CCUT = '1'), the CHAPS stops charging. During detection of accessories the charging is stopped to prevent, that 'high' charge current will disturb the sensible A/D-measurement.
Charging block diagram is shown in Figure overleaf.

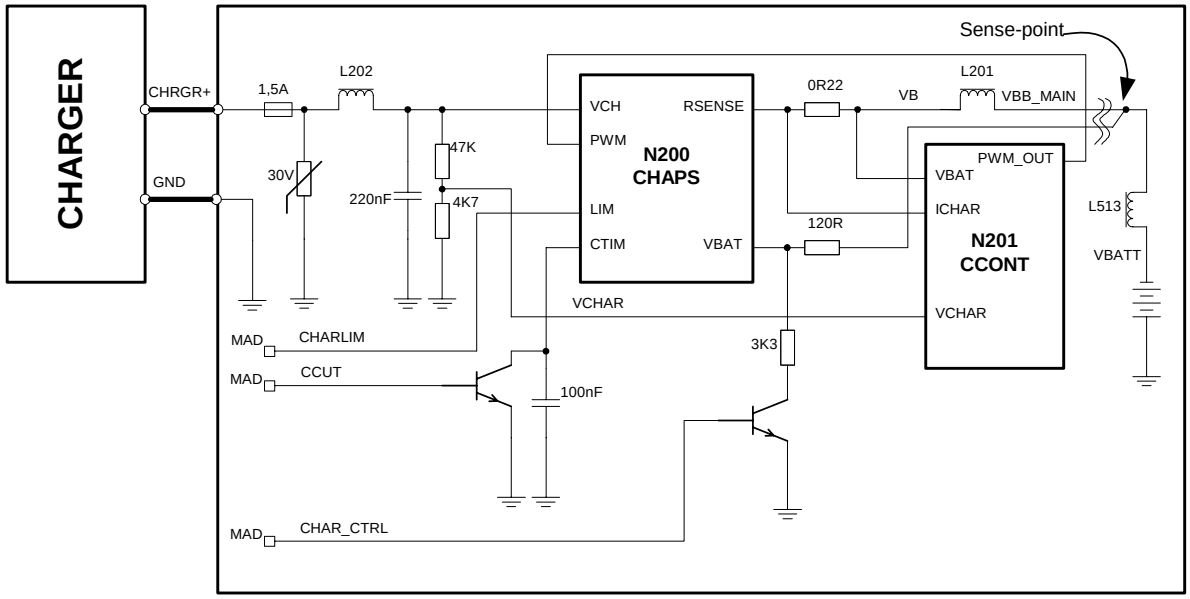


Figure 8: Charging Block Diagram

Start-up Charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial charging to a phone with an empty battery. Startup circuit charges the battery until the battery voltage level reaches 3.0V (+/- 0.1V) and the CCONT releases the PURX reset signal and program execution starts. Charging mode is changed from startup charging to PWM charging that is controlled by the MCU software.

If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken control over the charging, the startup current is switched off.
The startup current is switched on again when the battery voltage has dropped 100mV (nominal).

Table 8: Startup Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VOUT Start- up mode cutoff limit	Vstart	3.45	3.55	3.75	V
VOUT Start- up mode hysteresis NOTE: Cout = 4.7 uF	Vstarthys	80	100	200	mV
Start-up regulator output current VOUT = 0V ... Vstart	Istart	130	165	200	mA

Battery over-voltage protection

The CHAPS includes an over-voltage protection circuit (input pin VBAT), which purpose is to protect the phone from damage caused by too high Battery voltage.
Different cutoff voltages (VLIM1 or VLIM2) for two different battery types (Li or Ni) are selected by the MAD via CHAPS-input pin LIM according to the table below.

Table 9: VLIM Characteristics

Parameter	Symbol	LIM input	Min	Typ	Max	Unit
Output voltage cutoff limit (during transmission or Li-battery)	VLIM1	LOW	4.4	4.6	4.8	V
Output voltage cutoff limit (Ni-battery)	VLIM2	High	4.8	5.0	5.2	V

The internal power switch is immediately turned OFF, if the voltage at CHAPS-input pin VBAT rises above the selected limit VLIM.
When the internal power switch has turned OFF because of an overvoltage detection, it stays OFF until the Charger-voltage drops below Vpor (CHAPS Power On Reset Threshold) ($Vpor_{min.}$ = 2.8V, $Vpor_{max.}$= 3.12V). It is necessary to reconnect the charger to reset the VLIM protection.

The VBAT input of the CHAPS is connected through a 120R resistor to the battery voltage at a sense point close to the battery (see fig.9). A 1uF Capacitor is placed at the VBAT pin close to the CHAPS and acts with the 120R resistor as a filter to reduce influences of fast overvoltage transients caused by the Charger Switch or when connecting the charger.

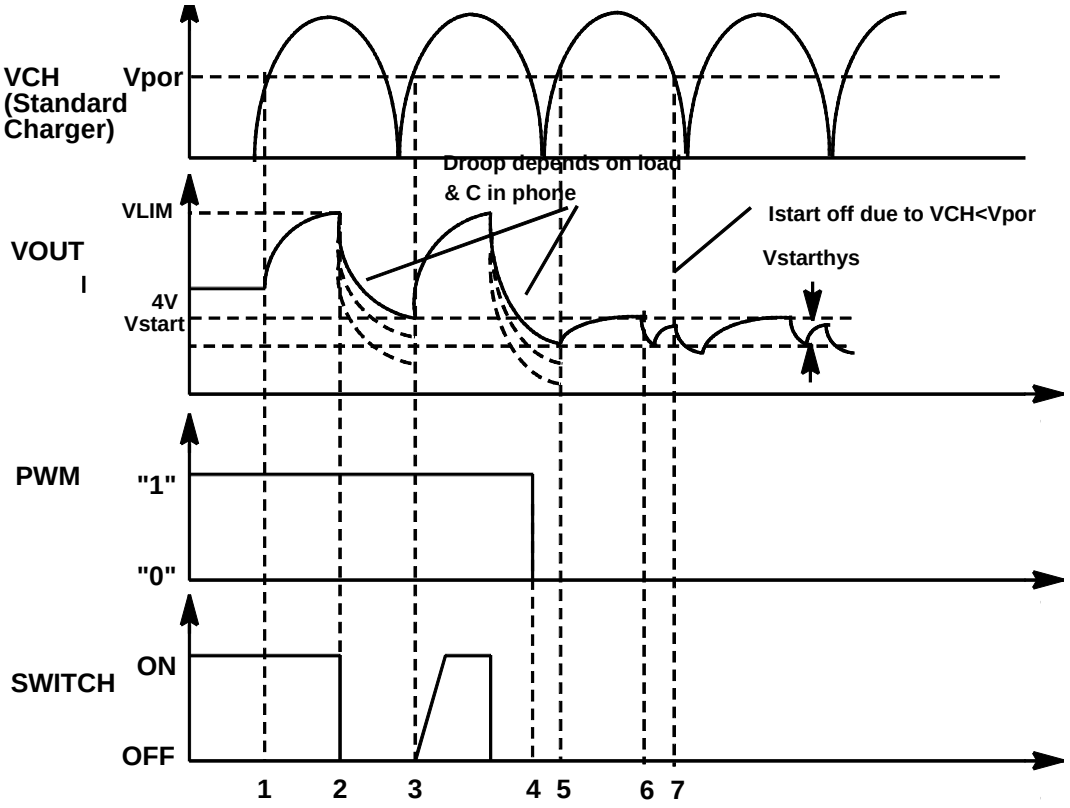
The newer battery types from the battery vendors are getting 'better and better', which means that the charge voltage of a fully charged battery now is higher than when the VLIM threshold was specified.
This means that the difference between VLIM and the actually battery voltage is decreasing and the risk of Overvoltage protection occur during a normal charge is likely to occur.
A voltage divider (120R + 3K3) on the VBAT input of the CHAPS is implemented to solve this problem. The voltage divider is only active during charging which is controlled by a transistor activated by the MAD signal CHAR_CTRL.
The voltage divider reduces the Sense voltage by approx. 175mV +/-25mV, which gives new values for VLIM as shown below :

$VLIM2_{min}$ = 4.8+0.175-0.025 = 4.95V
$VLIM2_{max}$ = 5.2+0.175+0.025 = 5.4V

Battery removal during charging

Output over-voltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

With a charger connected, if VOUT exceeds VLIM, CHAPS turns switch OFF until the charger input has sunken below Vpor (Vpor $_{min.}$ = 2.8V, Vpor $_{max.}$= 3.12V). MCU software will stop the charging (turn off PWM) when it detects that battery has been removed.



1. **Battery removed, (standard) charger connected, VOUT rises (follows charger**
2. **VOUT exceeds limit VLIM(X), switch is turned immediately**
3. **VOUT falls (because no battery) , also VCH<Vpor (standard chargers full-output). When VCH > Vpor and VOUT < VLIM(X) -> switch turned on again (also is still HIGH) and VOUT again exceeds**
4. **Software sets PWM = LOW -> CHAPS does not enter PWM**
5. **PWM low -> Startup mode, startup current flows until Vstart limit**
6. **VOUT exceeds limit Vstart, Istart is**
7. **VCH falls below**

Figure 9: Output Overvoltage protection - Battery Removed

PWM

When a charger is used, the power switch is turned ON and OFF by the PWM input. PWM rate is 1Hz. When PWM is HIGH, the switch is ON and the output current Iout = charger current - CHAPS supply current. When PWM is LOW, the switch is OFF and the output current Iout = 0. Soft switching is used to prevent the switching transients inducing noise in audio circuitry of the phone.

Battery identification (BSI)

Different battery types are identified by a pull-down resistor inside the battery pack. In the baseband area of the transceiver, the BSI line has a 150k pull-up to VBB. The MCU can identify the battery by reading the BSI line DC-voltage level with a CCONT (N201) A/D-converter.

Table 10: Battery Identification

Name	Min	Typ	Max	Unit	Notes
BSI	0		2,85 (VBB)	V	**B**attery **S**ize **I**ndication pull-up to VBB = 150k ± 5% SIM Card removal detection Treshold = 2.4V@VBB=2.8V
RS	-1%	3,3	+1%	Kohm	Indication resistor for BMC-2 battery (640mAh, NiMH)
Rs	-1%	5,6	+1%	Kohm	Indication resistor for BMC-3 battery (900mAh, NiMH)
Rs	-1%	75	+1%	Kohm	Indication resistor for BLC-2 battery (900mAh, 4.2v Lilon)
Rs	-1%	22	+1%	Kohm	Indication resistor for service battery

Note: *No support of 4.1v lithium*

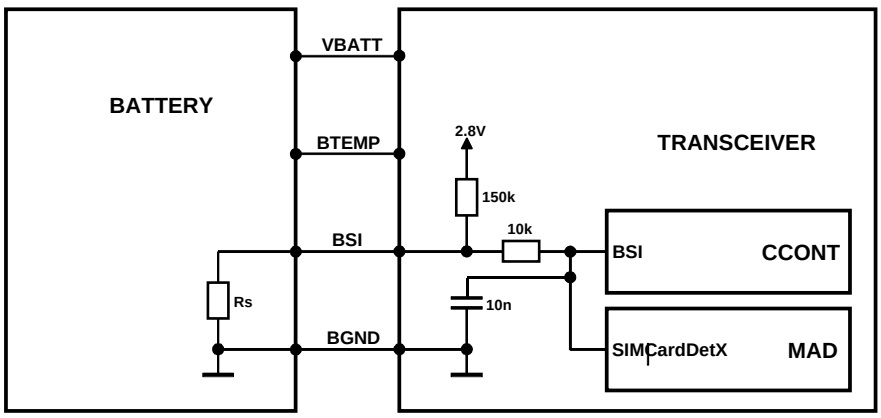


Figure 10: BSI Connections - All Batteries

The battery identification line is used also for battery removal detection. The BSI line is connected to a SIMCardDetX line of MAD2. SIMCardDetX is a threshold detector with a nominal input switching level 0.85xVcc for a rising edge and 0.55xVcc for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The BSI contact in the battery contact disconnects before the other contacts so that there is a delay between battery removal detection and supply power off.

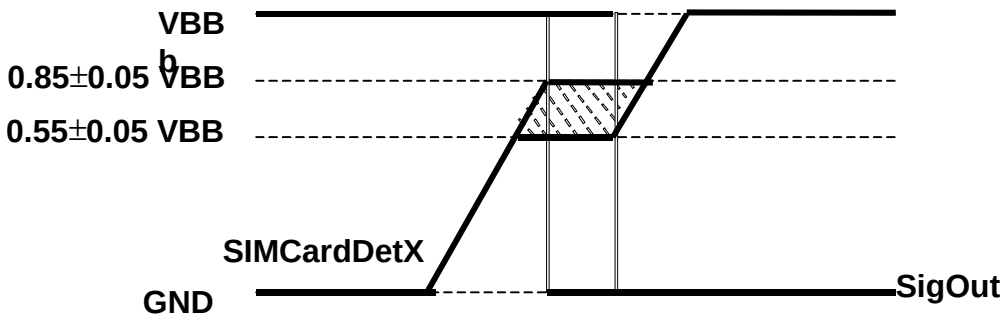


Figure 11: SIMCardDetX Detection Levels

Battery temperature (BTEMP)

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line inside transceiver has a 100k pull-up to VREF. The MCU calculates the battery temperature by reading the BTEMP line DC-voltage level with a CCONT (N201) A/D-converter.

Table 11: Battery Temperature

Name	Min	Typ	Max	Unit	Notes
BTEMP	0		VREF	V	Battery temperature indication 100k pull-up resistor to VREF in phone Battery package has NTC pull down resistor: 47kΩ. +/-5%@+25°C , B=4050+/-3%
	2.1 5	 10	3 20	V ms	IBI-pulse,Phone power up by battery (input) Power up pulse width
	-5		5	%	100k pull-up resistor tolerance

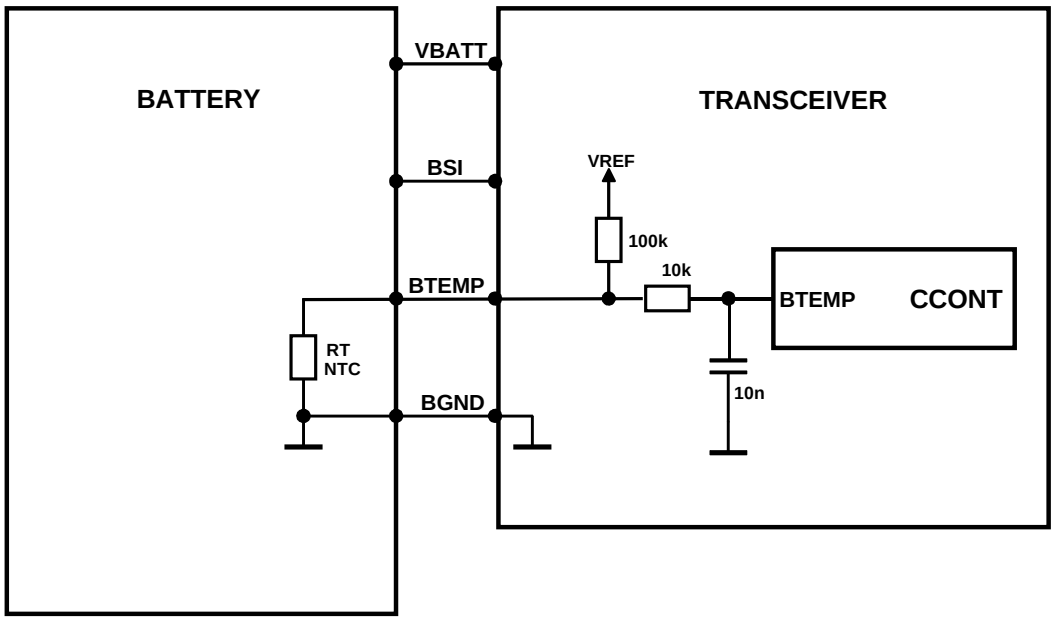


Figure 12: Standard Battery, BTEMP Connection

Supply voltage regulators

The heart of the power distribution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD2WD1 and memories, COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for the SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD2WD1 to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA. The CCONT supplies also 5V for RF.

Table 12: Regulator Activity - Different Operating Modes

Operating mode	Vref	RF REG	VCOBBA	VCORE	VBB	VSIM	SIMIF
Power off	Off	Off	Off	Off	Off	Off	Pull down
Power on	On	On/Off	On	On	On	On	On/Off
Reset	On	Off VR1 On VR6 On	On	On	On	Off	Pull down
Sleep	On	On/Off	Off	Off	On	On	On/Off

CCONT includes also five additional 2.8V regulators providing power to the RF section. These regulators are controlled by SW via the serial Bus GENSIO(1:0) from the MAD2WD1.

CCONT generates also a 1.5 V reference voltage VREF to COBBA. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

Switched mode power supply VSIM

There is a switched mode supply for SIM-interface. SIM voltage is selected via serial IO. The 5V SMR can be switched on independently of the SIM voltage selection, but can't be switched off when VSIM voltage value is set to 5V.

Table 13: Electrical Characteristics of VSIM and V5V

Characteristics	Condition	Min	Typ	Max	Unit
Output voltage VSIM	Over temperature Over current	2.8 4.8	3.0 5.0	3.2 5.2	V
Output voltage V5V	Over temp & current	4.8	5.0	5.2	V
Output voltage V5V_2	Over temperature	5.0		6.0	V
Output current VSIM	Continuous DC			30	mA
Output current V5V	Continuous DC			30	mA
current consumption VSIM	on sleep		200 100	330 150	uA uA

Note: *VSIM and V5V together can supply a total of 30mA.*

SMR / VSIM-functions is shown below.

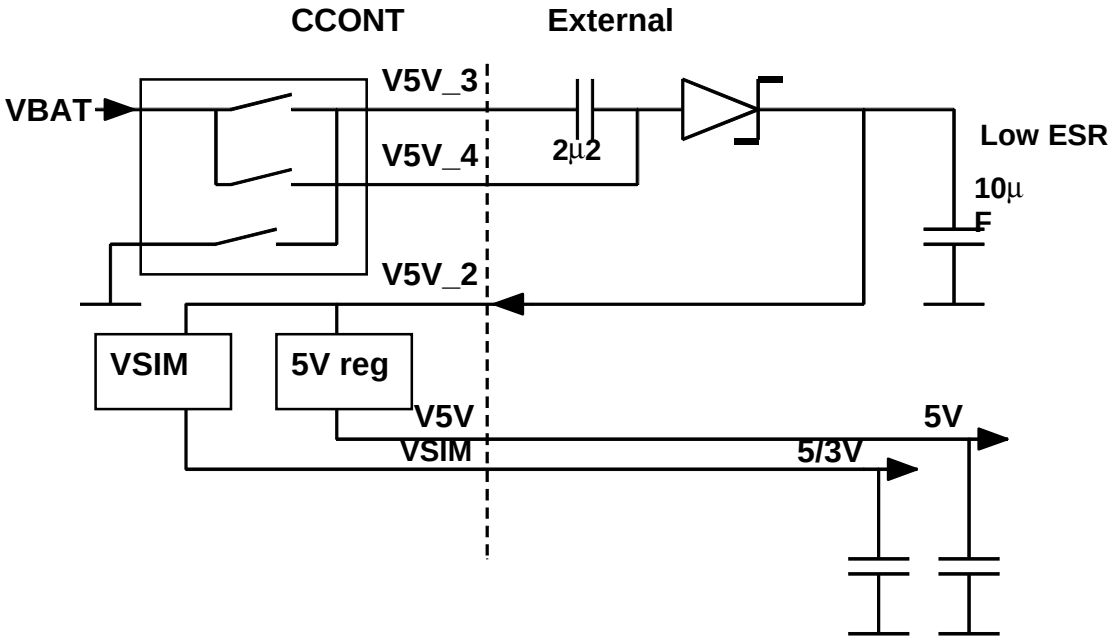


Figure 13: SMR Power Functions

Power Up and Power Down

When the PURX reset is released, the MAD2WD1 releases the System-reset signals (Ext-SysResetX and the internal MCUResetX) and starts the boot program execution.
The logic-level on the GenSDIO pin of the MAD2WD1 select where the BOOT program execution starts:

GenSDIO = '0' : from MAD2WD1 boot-ROM
GenSDIO = '1' : from external memory.

In normal operation, the program execution continues from the flash program memory. However, If the MBUS line is pulled low during the power up, then the boot-ROM starts a flash programming sequence and waits for the prommer response through FBUS_RX line.

The baseband is powered up by:

1 Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.

2 Pressing the power key, that generates a PWRONX signal from the power key to the CCONT, this starts the power up procedure.

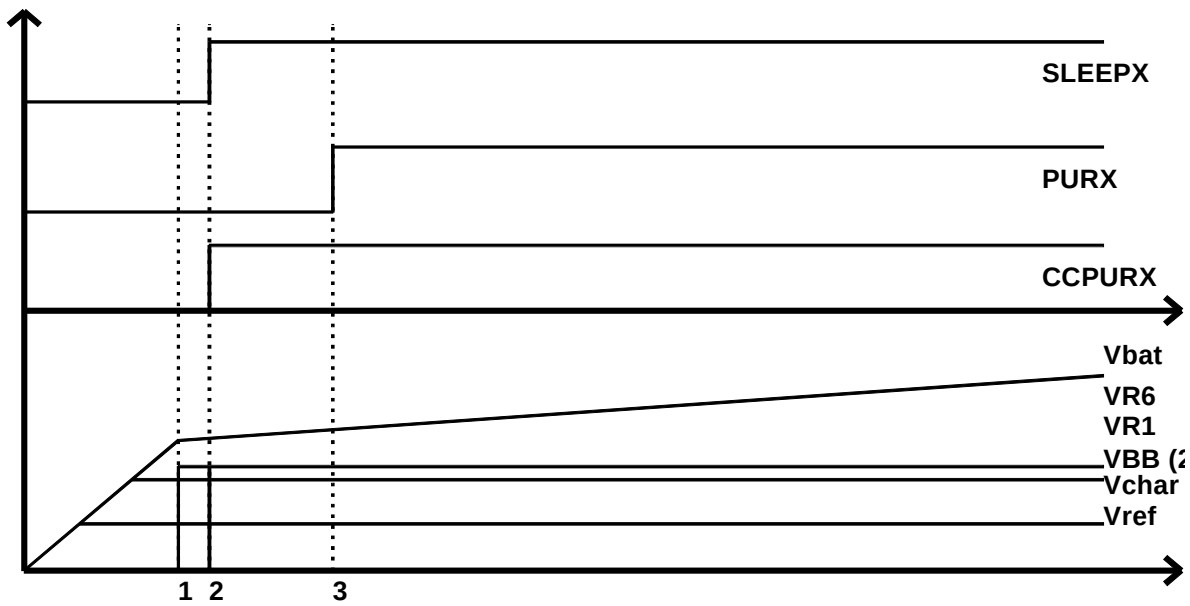
3 A RTC interrupt. If the real time clock is set to alarm and the phone is switched

off, the RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is connected to the PURX line to give a power on signal to the CCONT just like the power key.

4 IBI-pulse. When a short (10ms) voltage pulse is applied to the BTEMP pin, the CCONT wakes up and starts the power on procedure. This is used by the HDa12 Service tools.

Power up with a charger

When the charger is connected, CCONT will switch on the CCONT digital voltage as soon as the battery voltage exceeds 3.0V. The reset for CCONT's digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). Operating voltage for VCXO is also switched on. The counter in CCONT digital section will keep MAD2WD1 in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay, MAD2WD1 reset is released, and VCXO -control (SLEEPX) is given to MAD. The next diagram explains the power on procedure with charger (the picture assumes empty battery, but the situation would be the same with full battery):



1: Battery voltage over 3.0==>Digital voltages to CCONT
2: CCONT digital reset released. VCXO turned on
3: 62ms delay before PURX

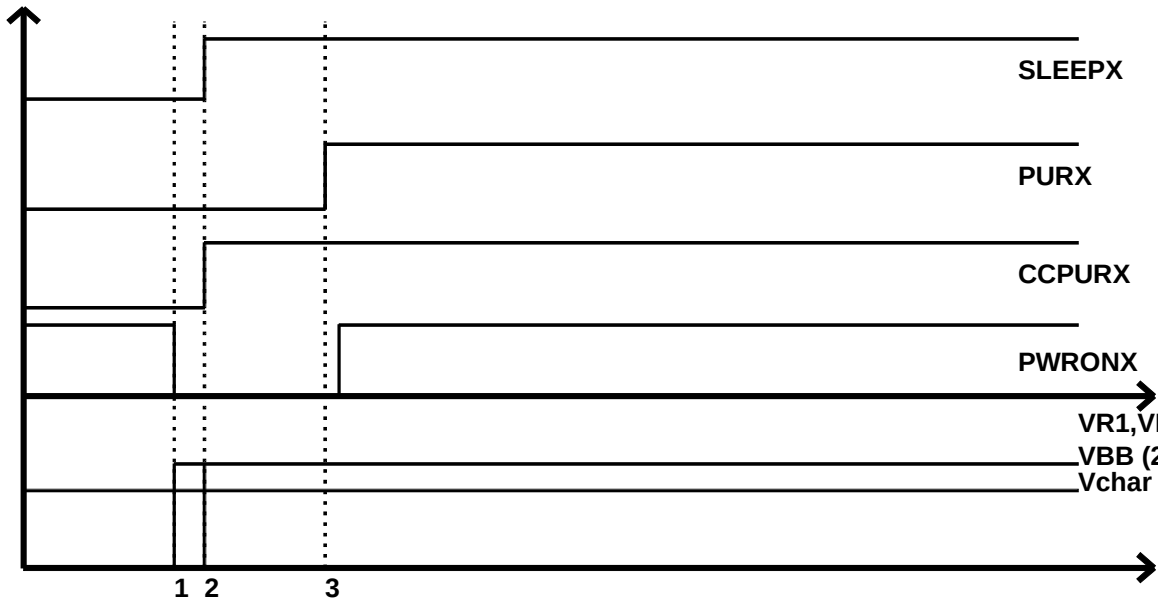
Figure 14: Power Up with Charger

When the phone is powered up with an empty battery pack using the standard charger,

the charger may not supply enough current for standard power-up procedure and the power-up is delayed.

Power up with power switch (PWRONX)

When the power on switch is pressed the PWRONX signal will go low. CCONT will switch on the CCONT digital section and VCXO, as was the case with the charger driven power up. If PWRONX is low when the 62 ms delay expires, PURX is released and SLEEPX control goes to MAD. If PWRONX is not low when 62 ms expires, PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts)



1: Power switch pressed ==> Digital voltages on in CCONT.
2: CCONT digital reset released. VCXO turned on.
3: ≈ 62 ms delay.

Figure 15: Power Up with Switch

Power up by RTC

When Alarm is selected by the user, and the phone is powered off, the RTC (internal in CCONT) will power up the phone at the alarm set time (internal CCONT signal RTCPwr set to logical 1).

Power up by IBI

IBI can power CCONT up by giving a short pulse (10ms) through the BTEMP line. After power-up BTEMP will act as any other input channel for ADC.

Power Down

The baseband is powered down by:

- Pressing the power key, that is monitored by the MAD, which starts the power down procedure.
- If the battery voltage is dropped below the operation limit, either by not charging it or by removing the battery.
- Letting the CCONT watchdog expire, which switches off all CCONT regulators and the phone is powered down.
- Setting the real time clock to power off the phone by a timer. The RTC generates an interrupt signal, when the alarm is turned off by the user. The RTC interrupt signal is connected to the PWRONX line to give a power off signal to the CCONT just like the power key.

The power down is controlled by the MAD. When the power key has been pressed long enough, or the battery voltage is dropped below the limit, the MCU initiates a power down procedure and disconnects the SIM power. Then the MCU outputs a system-reset signal and resets the DSP. If there is no charger connected the MCU writes a short delay to CCONT watchdog and resets itself. After the set delay the CCONT watchdog expires, which activates the PURX and all regulators are switched off and the phone is powered down by the CCONT.

Modes of Operation

Acting Dead

If the phone is off or switched off when the charger is connected, the phone is powered on but enters a state called "acting dead". To the user, the phone acts as if it was switched off. A battery-charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several sub-states in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc.

Sleep Mode

In the sleep mode all the regulators except the baseband VBB and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD2WD1 after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off and the VCXO power control, VCXOPwr is set low. In this state, only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the ExtSysResetX signal, and the flash is deep powered down during the sleep mode.

The sleep mode is exited either by the expiration of a sleep clock counter in the MAD2WD1 or by some external interrupt, generated by a charger connection, key press, headset connection etc. The MAD2WD1 starts the wake up sequence and sets the VCXOPwr and ExtSysResetX control high. After VCXO settling-time other regulators and clocks are enabled for active mode. If the battery pack is disconnected during the sleep mode, the CCONT pulls the SIM interface lines low as there is no time to wake up the MCU.

Charging

Charging is allowed in any operating mode. For Ni-MH batteries the max. charging temperature is +48°C. Above this temperature the charging algorithm is changed to 'hot-charge' which means that only the amount of current that is taken out from the battery is charged at the same time to the battery.

The battery type/size is indicated by a resistor inside the battery pack. The resistor value corresponds to a specific battery capacity. This capacity value is related to the battery technology as different capacity values are achieved by using different battery technology.

The battery voltage, temperature, size and current are measured by the CCONT controlled by the EM-software (Energy Management) running in the MAD.

The Energy-Management controls the charging current delivered from the charger to the battery. Charging is controlled by a PWM input signal, generated by the CCONT. The PWM pulse width is controlled by the MAD2WD1 and sent to the CCONT through a serial data bus. The battery voltage rise is limited by turning the CHAPS switch off when the battery voltage has reached 5.2V. Charging current is monitored by measuring the voltage drop across a 220 mOhm resistor.

Watchdog

The Watchdog block inside CCONT contains a watchdog counter and some additional logic, which are used for controlling the power on and power off procedures of CCONT. Watchdog output is disabled when WDDisX pin is tied low, - the WD–counter runs during that time, though. Watchdog counter is reset internally to 32 sec. at power up.
It is reset by the MAD2WD1 when writing a control word to the WDReg. in the CCONT.

Audio Control

PCM serial interface

The interface consists of following signals: a PCM codec master clock (PCMDClk), a frame synchronization signal to DSP (PCMSClk), a codec transmit data line (PCMTX) and a codec receive data line (PCMRX). The COBBA-GJP generates the PCMDClk clock, which is supplied to DSP SIO. The COBBA-GJP also generates the PCMSClk signal to DSP by dividing the PCMDClk. The PCMDClk frequency is 520 KHz and is generated by dividing the RFIClk 13 MHz by 25. The COBBA-GJP further divides the PCMDClk by 65 to get aPCMSClk signal, 8.0 kHz.

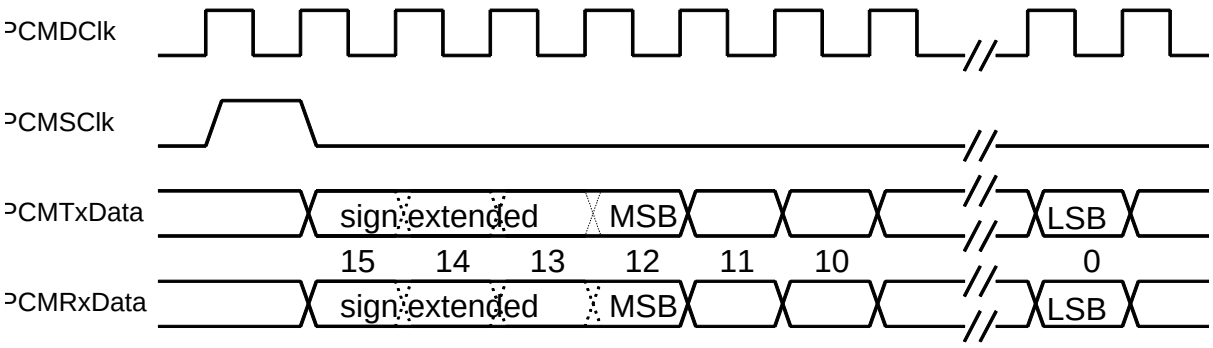


Figure 16: Audio Control Timimg Chart

Digital Control

The baseband functions are controlled by the MAD2WD1 ASIC (GSM/PCN specific), which consists of a MCU, a system ASIC and a DSP.

MAD2WD1

MAD2WD1 contains following building blocks:

ARM RISC processor with both 16-bit instruction set (THUMB mode) and 32-bit instruction set (ARM mode)

TI Lead DSP core with peripherals:

- API (Arm Port Interface memory) for MCU-DSP communication, DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting.
- Serial port (connection to PCM)
- Timer
- DSP memory

BUSC (Bus Controller for controlling accesses from ARM to API, System Logic and MCU external memories, both 8- and 16-bit memories)

System Logic

- CTSI (Clock, Timing, Sleep and Interrupt control)
- MCUIF (Interface to ARM via BUSC). Contains MCU Boot-ROM
- DSPIF (Interface to DSP)
- MFI (Interface to COBBA AD/DA Converters)
- CODER (Block encoding/decoding and A51&A52 ciphering)
- AccIF(Accessory Interface)
- SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)
- UIF (Keyboard interface, serial control interface for COBBA PCM Codec, LCD Driver and CCONT)
- SIMI (SimCard interface with enhanced features)
- PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)
- Flexpool

The MAD2WD1 operates from a 13 MHz system clock, which is generated by an internal 'divide by 2' circuit in the HAGAR RF-ASIC. Input to the HAGAR divider is from the 26Mhz VCXO frequency. The MAD2WD1 supplies a 13 MHz internal clock for the MCU and system logic blocks and a 13 MHz clock for the DSP, where it is multiplied to 45.5 MHz DSP clock (13MHz x 7/2).
The system clock is stopped in sleep-mode by disabling the VCXO supply from the CCONT regulator output (VR1). The CCONT provides a 32 kHz sleep clock for internal use and to the MAD2, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available i.e. always when the battery is connected.
MAD2WD1 supply voltages are VBB for I/O and VCORE for Internal functions as CPU, DSP and System Logic.

Table 14: Mad2WD1 Pin Connections

Ball	Name	Pin Type	Note	HDa12. ub4-11 Function
A1	MCUGENIO0	IO		CCUT (for CHAPS)
B1	SynthClk	O		SynthClk
C2	LEADGND0	PWR		GND
C1	DSPGenOut2	IO		Not Used
D4	Col2	IO	Pull up	Col2
D3	Col3	IO	Pull up	Col3
D2	Col4	IO	Pull up	Col4
D1	LCDCSX	IO		LCDEN
E4	GND0	PWR		GND
E3	Row5LCDCD	IO	Pull up	LCDCD
E2	Row4	IO	Pull up	Row4
E1	LEADVCC0	PWR		2.5V
F4	Row3	IO	Pull up	Row3
F3	Row2	IO	Pull up	Row2
F2	Row1	IO	Pull up	Row1 (power key)
F1	Row0	IO	Pull up	Not Used
G2	MCUAd21	IO	Pull up	Not Used
G1	VCCSYS0	PWR		2.5V
G3	MCUAd20	IO	Pull down	MCUAd20
G4	MCUAd19	O		MCUAd19
H1	VCCIO0	PWR		2.8V
H2	MCUAd18	O		MCUAd18
H3	MCUAd17	O		MCUAd17
H4	LEADGND1	PWR		GND
J1	MCUAd16	O		MCUAd16
J2	MCUAd15	IO		MCUAd15
J3	MCUAd14	IO		MCUAd14
J4	GND1	PWR		GND
K1	MCUAd13	IO		MCUAd13
K2	MCUAd12	IO		MCUAd12
K3	MCUAd11	IO		MCUAd11
L1	ARMGND	PWR		ARMGND
L2	MCUAd9	IO		MCUAd9
L3	MCUAd8	IO		MCUAd8
M1	MCUAd6	IO		MCUAd6
M2	MCUAd5	IO		MCUAd5

Ball	Name	Pin Type	Note	HDa12. ub4–11 Function
N1	MCUAd2	IO		MCUAd2
N2	MCUAd1	IO		MCUAd1
M3	MCUAd4	IO		MCUAd4
N3	MCUAd0	IO		SRAM UB (Upper; 16 bit data)
K4	ARMVCC	PWR		2.5V
L4	MCUAd7	IO		MCUAd7
M4	MCUAd3	IO		MCUAd3
N4	VCCSYS1	PWR		2.5V
K5	MCUAd10	O		MCUAd10
L5	GND2	PWR		GND
M5	MCURdX	O		MCURdX
N5	MCUWrX	O		MCUWrX
K6	ExtMCUDa0	IO	Pull down	MCUDa0
L6	ExtMCUDa1	IO	Pull down	MCUDa1
M6	ExtMCUDa2	IO	Pull down	MCUDa2
N6	ExtMCUDa3	IO	Pull down	MCUDa3
M7	ExtMCUDa5	IO	Pull down	MCUDa5
N7	ExtMCUDa6	IO	Pull down	MCUDa6
L7	ExtMCUDa4	IO	Pull down	MCUDa4
K7	VCCIO1	PWR		2.8V
N8	ExtMCUDa7	IO	Pull down	MCUDa7
M8	MCUGenIODa0	IO	Pull down	MCUDa8
L8	MCUGenIODa1	IO	Pull down	MCUDa9
K8	MCUGenIODa2	IO	Pull down	MCUDa10
N9	MCUGenIODa3	IO	Pull down	MCUDa11
M9	MCUGenIODa4	IO	Pull down	MCUDa12
L9	MCUGenIODa5	IO	Pull down	MCUDa13
K9	GND3	PWR		GND
N10	MCUGenIODa6	IO	Pull down	MCUDa14
M10	VCCSYS2	PWR		2.5V
L10	MCUGenIODa7	IO	Pull down	MCUDa15
N11	ROM1SelX	O		ROM1SelX (F_CE)
M11	RAMSelX	O		RAMSelX (S_CS)
L11	JTDO	IO	Pull up	JTDO
N12	JTRst	IO	Pull down	JTRst
M12	JTClk	IO	Pull up	JTClk
N13	JTDI	IO	Pull up	JTDI
M13	JTMS	IO	Pull up	JTMS

Ball	Name	Pin Type	Note	HDa12. ub4-11 Function
L12	CoEmu0	IO	Pull up	CoEmu0
L13	CoEmu1	IO	Pull up	CoEmu1
K10	SCVCC	PWR		2.8V
K11	RFClk	X1		RFC
K12	RFClkGND	PWR		GND
K13	SIMCardDetX	X2		CARDDET
J10	SCGND	PWR		GND
J11	ROM2SelX	IO	Pull up	Not Used (MEMC(6))
J12	GND4	PWR		GND
J13	EEPROMSelX	IO	Pull up	BUTTON_CTRL
H10	LEADVCC1	PWR		2.5V
H11	MCUGenIO1	IO	Pull up	PA_Vendor1 (detect)
H12	Testmode	I	Pull down	Testmode
H13	ExtSysResetX	O		Flash_WP/_RP
G12	VibraPWM	IO	Pull down	Vibra
G13	VCCIO2	PWR		2.8V
G11	VCCSYS3	PWR		2.5V
G10	MCUGenIO4	IO	Pull up	CHARLIM
F13	LEADGND2	PWR		GND
F12	LoByteSelX	IO	Pull up	SRAM LB (Lower; 16 bit data)
F11	HookDet	IO		HookDet
F10	HeadDet	IO		HeadDet
E13	MCUGenIO2	IO	Pull up	PA_Vendor2 (detect)
E12	MCUGenIO3	IO	Pull up	KBLIGHTS
E11	VCXOPwr	O		VCXOPwr / SleepX
E10	GND5	PWR		GND
D13	SynthPwr	IO	Pull down	Not Used
D12	SIMCardPwr	IO	Pull up	SIMCardPwr
D11	LEADVCC2	PWR		2.5V
C13	RxPwr	IO	Pull down	Flash Vpp ctr. (protect)
C12	TxPwr	IO	Pull down	LCDLIGHTS
C11	SIMCardData	IO		SIMCardData
B13	PURX	I		PURX
B12	CCONTInt	I		CCONTInt
A13	Clk32k	I		SleepClk
A12	SIMCardClk	O		SIMCardClk
B11	SIMCardRstX	O		SIMCardRstX
A11	SIMCardIOC	O		SIMCardIOC

Ball	Name	Pin Type	Note	HDa12. ub4-11 Function
D10	VCCIO3	PWR		2.8V
C10	GenCCONTCSX	O		CCONTCSX
B10	GenSDIO	IO		GenSDIO
A10	GenSClk	O		GenSClk
D9	BuzzPWM	IO	Pull down	Buzzer
C9	GND6	PWR		GND
B9	PCMTxData	IO	Pull down	PCMTxData
A9	PCMRxData	IO	Pull up	PCMRxData
D8	DSPXF	IO	Pull up	Not Used / DSPXF
C8	PCMIO	IO	Pull up	Not used
B8	PCMDClk	IO	Pull down	PCMDClk
A8	PCMSClk	IO	Pull down	PCMSClk
B7	VCCSYS4	PWR		2.5V
A7	COBBASD	IO		SERRFI Serial Data
C7	Idata	IO	Pull up	SERRFI Idata
D7	Qdata	IO	Pull up	SERRFI Qdata
A6	COBBACSX	O		SERRFI CSX
B6	VCCIO4	PWR		2.8V
C6	COBBAClk	O		CobbaClk
D6	AccRxData	I		FBUS Rx
A5	DSPGenOut5	O		HAGAR_RESET_X
B5	MBUS	IO		MBUS
C5	AccTxData	IO		FBUS Tx
D5	GND7	PWR		GND
A4	DSPGenOut4	IO		COBBA_RESET_X
B4	SynthEna2X	IO	Pull down	CHAR_CTRL
C4	Col1	IO	Pull up	Col1
A3	FrACtrl	IO	Pull down	LCDRSTX
B3	SynthEna	O		SynthEna
C3	Col0	IO	Pull up	Col0
A2	TxPA	IO	Pull down	TXP / TXPwr (CCONT)
B2	SynthData	O		SynthData

Memory

The MCU program code resides in an external flash program memory, which size is 16Mbits (1024k x 16bit) for 3310 and 32 Mbits (2048k x 16bit) for 3330. The MCU work (data) memory size is 1024 kbits (64k x 16bit) for 3310 and 2048kbits (128k x 16bit) for 3330.

The Bus Controller (BUSC) section in the MAD2WD1 decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip-select signals. BUSC supports a programmable number of wait states for each memory range.

Program and Data Memory

The MCU program code resides in the program memory.

'3310' Program memory is 16Mbits (1024k x 16bit) Flash memory.
'3330' Program memory is 32Mbits (2048k x 16bit) Flash memory.

The flash memory has a power down pin, which is kept low, during the power up phase of the flash to ensure that the device is powered up in the correct state, read only. The power down pin is utilized in the system sleep mode by connecting the ExtSysResetX to the flash power down pin to minimize the flash power consumption during the sleep.

Nonvolatile data memory is implemented with program (Flash) memory. Special EEPROM emulation (EEEMmu) software is utilized.

Work Memory

The work memory is a static RAM of size 1024kbits (64k x 16) for 3310 and 2048kbits (128k x 16bit) for 3330. The memory contents are lost when the baseband voltage is switched off. All retainable data is stored in the data memory (Flash) when the phone is powered down.

MCU Memory Map

MAD2WD1 supports maximum of 4GB internal and 4MB external address space. External memories use address lines MCUAd0 to MCUAd21 and 8-bit/16-bit databus.
The BUSC bus controller supports 8- and 16-bit access for byte, double byte, word and double word data.

Access wait states may be set to 0, 1, 2 or 3. In HDa12, 1 Wait-state is selected.

Flash Programming

The phone has to be connected to the flash loading adapter so that supply voltage for the phone and data transmission lines can be supplied from/to the adapter. When adapter switches supply voltage to the phone, the program execution starts from the BOOT-ROM and the MCU investigates in the early start-up sequence if the flash prommer is connected. This is done by checking the status of the MBUS-line. Normally this

line is high but when the flash prommer is connected, the line is forced low by the prommer.

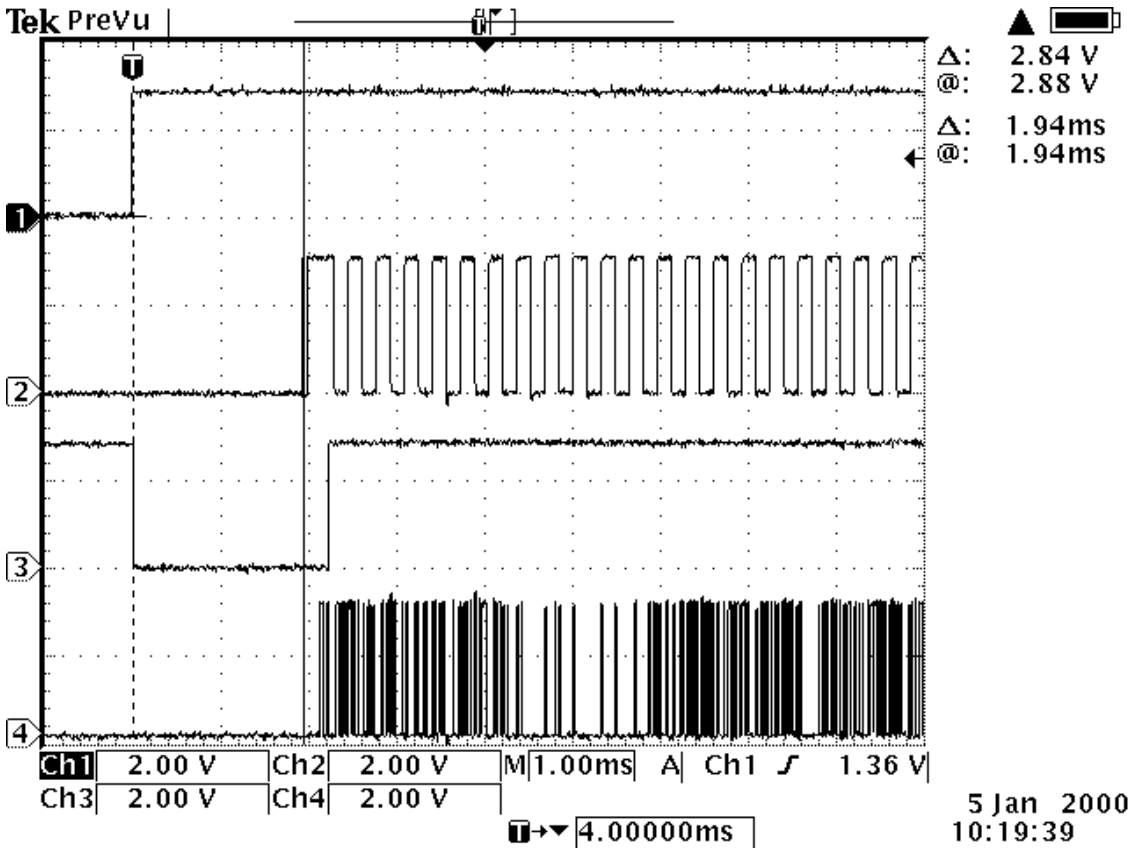
The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone. The data transmit line from the baseband to the prommer is initially high. When the baseband has recognized the flash prommer, the TX-line is pulled low. This acknowledgement is used to start to toggle MBUS (FCLK) line three times in order that MAD2 is initialized. This must happened within 15 ms after TX line is pulled low. After that, the data transfer of the first two bytes from the flash prommer to the baseband on the RX-line must be done within 1 ms.

When MAD2 has received the secondary boot byte count information, it forces TX line high. Now, the secondary boot code must be sent to the phone within 10 ms per 16 bit word. If these timeout values are exceeded, the MCU (MAD2) starts normal code execution from flash. After this, the timing between the phone and the flash prommer is handled with dummy bites.

The Flash Program Voltage (VPP) is either internal (VBB= 2.8V) or +12V from an external voltage supply.
+12V VPP is only to be used in the factory by the FLALI- and Label- Stations. +12V VPP is not an option for service tools.

Table 15: Flash Programming Timing Characteristics

Characteristics	Max	Unit
Time from boot indication to MAD2 initialization sequence	15	ms
Time from MAD2 initialization sequence to byte lenght information	1	ms
Time from byte lenght information to end of secondary boot code loading.	10 per16 bit word	ms



Ch1: PURX (R307)	Ch3: F_Tx (X202, pin7)
Ch2: Mbus (X202, pin 3)	Ch4: F_Rx (X202, pin 8)

Figure 17: Flash Programming Sequence

Flash Protection/ +12V VPP

+2.8V programming (internal):

At +2.8V Programming the Vpp input of the Flash (ref. D301) is controlled by the MAD2WD1 as a write enable signal. The MAD2WD1 will control EEPROM access and all reprogramming in After Sales (HDa12 Service tools).

The purpose of the 3.0V Voltage Detector D300 is to guarantee no writing to the Flash if the Battery voltage is insufficient (< 3.0V).
If VB< 3.0V, then the Open drain FET output of the detector shorts, and by this inhibit the MAD2WD1 to generate VPP (write enable) to the Flash.

+12V programming (external):

+12V Flash is used in the production (FLALI, FINUI and Label-station) to speed up programming.
A FET grounds the VPP_GND terminal in the Production-Jig as soon as the +12V is detected on Vpp. This protects the MAD2WD1 VPP-output (ball C3) from the external +12V voltage source.

+12V is applied directly to the VPP terminal of the Flash, which then act as a power-supply input.
After the programming sequence, VPP will float in the test jig and thus enables the MAD2WD1 to control writing to the emulated EEPROM

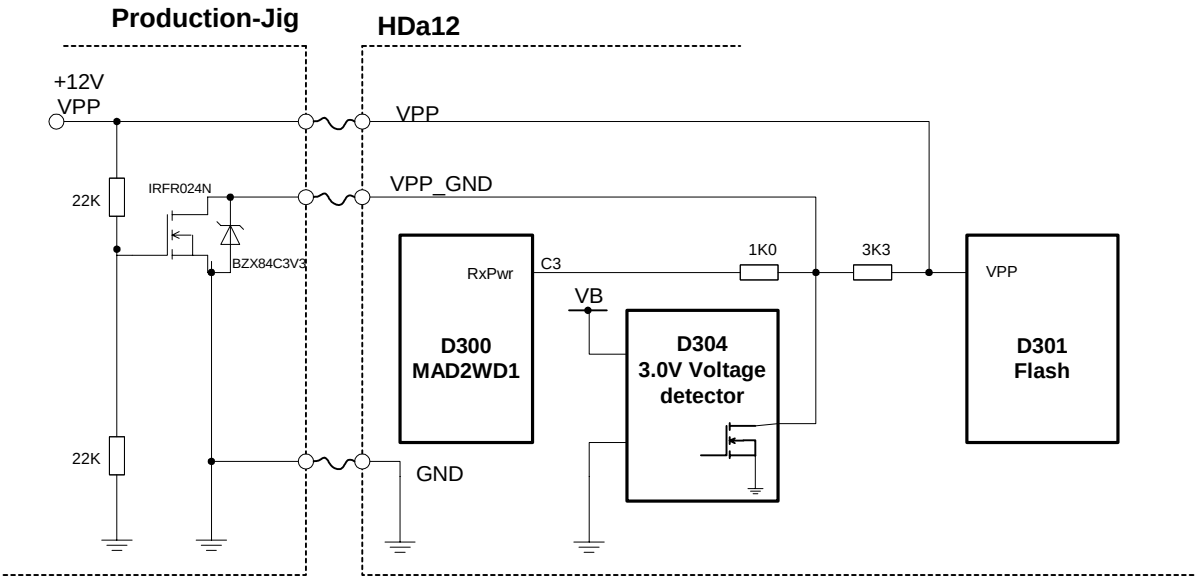


Figure 18: Flash Protection/ +12V Flash

COBBA GJP

COBBA GJP ASIC provides an interface between the baseband and the RF-circuitry. COBBA performs analogue to digital conversion of the receive signal. For transmit path COBBA performs digital to analogue conversion of the 'Transmit Amplifier Power Control Ramp' and the In-phase and Quadrature signals. A slow speed digital to analogue converter will provide automatic frequency control (AFC).

COBBA is at any time connected to MAD2WD1 asic with two interfaces, one for transferring TX and RX data between MAD2WD1 and COBBA and one for transferring codec RX/TX samples.

Real time clock

Requirements for a Real Time Clock (RTC) implementation are a basic clock (hours and minutes), a calendar and a timer with alarm and power on/off -function and miscellaneous calls. The RTC will contain only the time base and the alarm timer but all other functions (e.g. calendar) are implemented with the MCU software.

The RTC is integrated in the CCONT, because the CCONT already contains the power up/down functions and a 32kHz sleep-clock, which is always running when the phone battery is connected. The 32 KHz sleep-clock is used as time source to a RTC block.

RF Module

This RF module takes care of all RF functions of EGSM/DCS1800 dualband engine. RF circuitry is located on one side of the 8-layer transceiver-PCB. PCB area for the RF circuitry is about 15 cm2. The RF design is based on the dualband direct conversion RF-IC "Hagar". There is no intermediate frequency and that means the number of component is much lower than before and therefore much less interference problems than previously.

EMC emissions are taken care of using metal shielding cans, which screens the whole transceiver. Internal screening is realized by separating different sections of the RF by shielding cans. The VCO is isolated from Hagar and external components by a can in the Hagar shielding can and PA, RX/TX Switch and LNA's are located in a separate can. The baseband circuitry is located on the same side of the same board, but in a separate shielding can.

Maximum Ratings

Table 16: RF max ratings

Parameter	Rating
Battery voltage, idle mode	5.2 V (charging)
Regulated supply voltage	2.8 +/- 3% V
Voltage reference	1.5 +/- 1.5% V
Operating temperature range	-10...+55 deg. C
Absolute maximum battery voltage	4.2 V (charging)

RF Characteristics

Table 17: RF Characteristics

Item	Values (EGSM / DCS1800)
Receive frequency range	925 ... 960 MHz / 1805 ... 1880 MHz
Transmit frequency range	880 ... 915 MHz / 1710 ... 1785 MHz
Duplex spacing	45 MHz / 95 MHz
Channel spacing	200 kHz
Number of RF channels	174 / 374
Power class	4 (EGSM900) / 1 (DCS1800)
Number of power levels	15 / 16

RF Frequency Plan

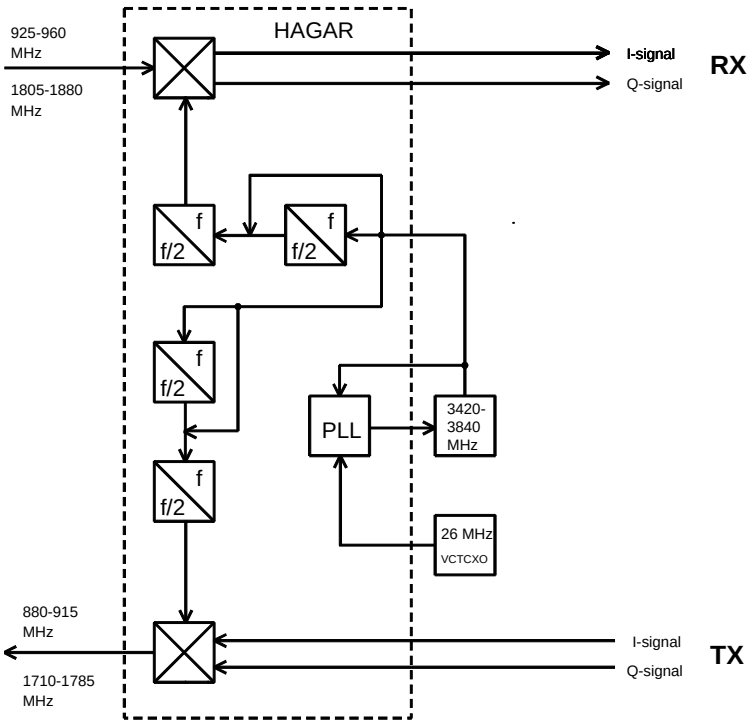


Figure 19: RF Fequency Plan

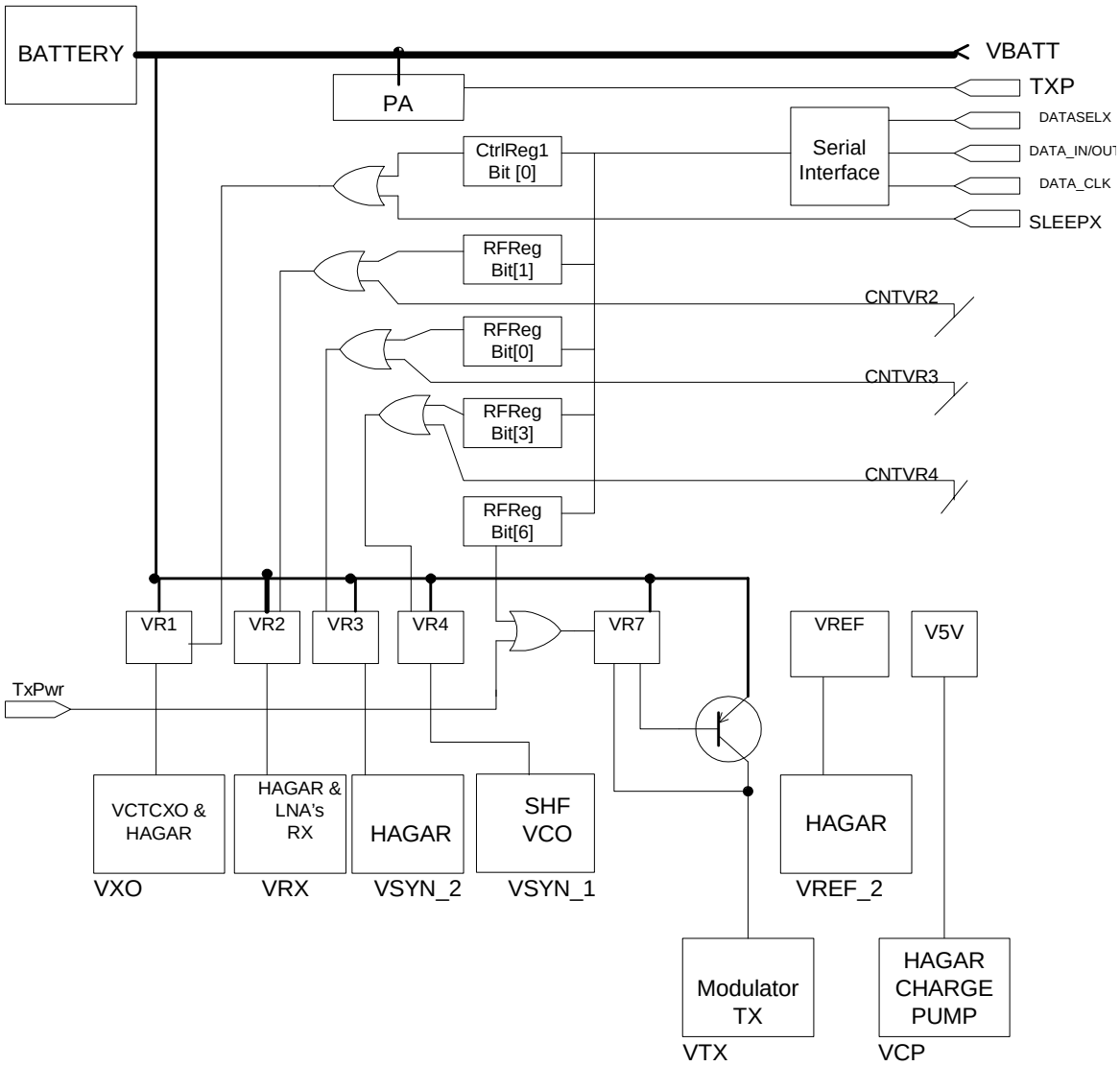
DC characteristics

Regulators

Transceiver has a multi function power management IC at baseband section, which contains among other functions, also 7 pieces of 2.8 V regulators. All regulators can be controlled individually with 2.8 V logic directly or through control register.

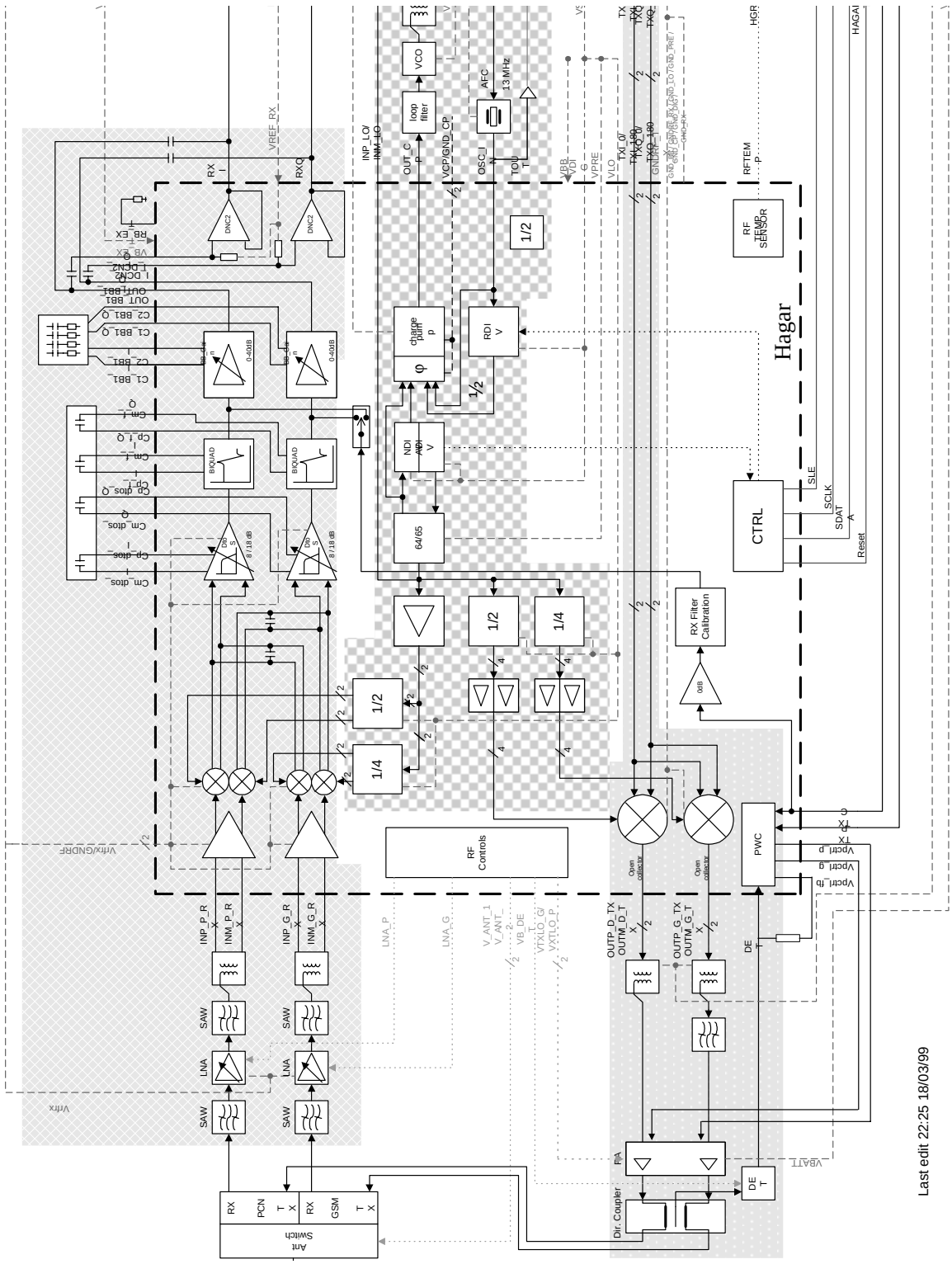
VREF from CCONT IC and VREF RX from COBBA IC are used as the reference voltages for HAGAR RF-IC, VREF (1.5V) for bias reference and VREF RX (1.2V) for RX ADC's reference.

Power Distribution Diagram



RF Functional Description-Diagram

Architecture contains one RF-IC, dualband PA module, VCO-module, VCTCXO module and discrete LNA stages for both receive bands.



Frequency Synthesizer

VCO frequency is locked with PLL into stable frequency source, which is a VCTCXO-module (voltage controlled temperature compensated crystal oscillator). VCTCXO is running at 26 MHz. Temperature effect is controlled with AFC (Automatic Frequency Control) voltage. VCTCXO is locked into frequency of the base station. AFC is generated by baseband with an 11 bit conventional DAC in COBBA.

PLL is located in HAGAR RF-IC and is controlled via serial bus from COBBA-IC (baseband).

There are 64/65 (P/P+1) prescaler, N- and A-divider, reference divider, phase detector and charge pump for the external loop filter. SHF local signal, generated by a VCO-module (VCO = voltage controlled oscillator), is fed to prescaler. Prescaler is a dual modulus divider. Output of the prescaler is fed to N- and A-divider, which produce the input to phase detector. Phase detector compares this signal to reference signal (400kHz), which is divided with reference divider from VCTCXO output. Output of the phase detector is connected into charge pump, which charges or discharges integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency.

Loop filter filters out the pulses and generates DC control voltage to VCO. Loop filter defines step response of the PLL (settling time) and effects to stability of the loop, that's why integrator capacitor has got a resistor for phase compensation. Other filter components are for sideband rejection. Dividers are controlled via serial bus. SDATA is for data, SCLK is serial clock for the bus and SENA1 is a latch enable, which stores new data into dividers.

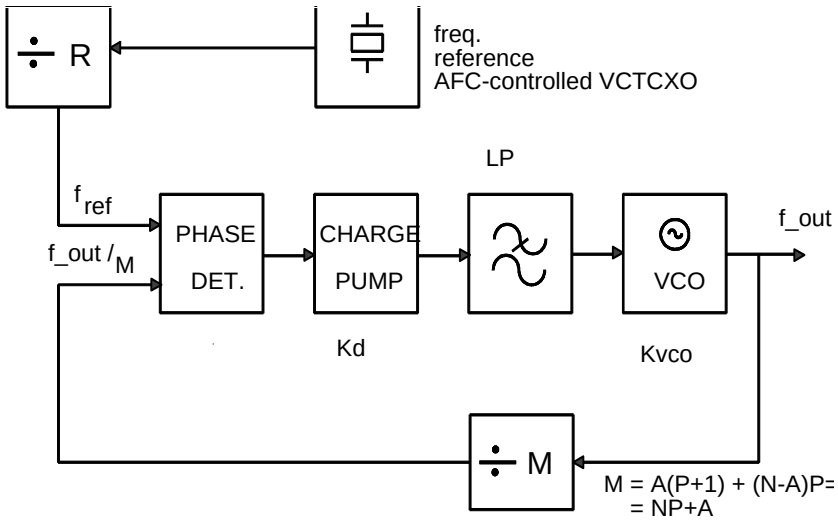


Figure 20: Frequency Synthesiser

LO-signal is generated by SHF VCO module. VCO has double frequency in DCS1800 and x 4 frequency in EGSM compared to actual RF channel frequency. LO signal is divided by two or four in HAGAR (depending on system mode).

Receiver

The receiver is a direct conversion, dualband linear receiver. Received RF-signal from the antenna is fed via RX/TX switch to 1st RX SAW filter and LNA's (low noise amplifier), separate branches for EGSM900 and DCS1800. Gain selection control of LNA's comes from HAGAR IC. Gain step is activated when RF-level at the antenna is about -45 dBm.

After the LNA the amplified signal (with low noise level) is fed to bandpass filter (2nd RX SAW filter). RX bandpass filters defines how good supperssion of blocking signals outside receive band and the protection against spurious responses.

After the bandpass filters the signals are fed to baluns which converts the single ended signal to ballanced. The balanced signal is fed to the RF input of Hagar. Differential RX signal is amplified and mixed directly down to BB frequency in HAGAR. Local signal is generated with external VCO. VCO signal is divided by 2 (DCS1800) or by 4 (EGSM900). PLL and dividers are in HAGAR-IC.

From the mixer output to ADC input RX signal is divided into I- and Q-signals. Accurate phasing is generated in LO dividers. After the mixer DTOS amplifiers convert the differential signals to single ended. DTOS has two gain stages. The first one has constant gain of 12dB and 85kHz cut off frequency. The gain of second stage is controlled with control signal g10. If g10 is high (1) the gain is 6dB and if g10 is low (0) the gain of the stage is -4dB.

The active channel filters in HAGAR provides selectivity for channels (-3dB @ +/-100 kHz typ.). The integrated base band filter is an active-RC-filter with two off-chip capacitors. Large RC-time constants are needed in the channel select filter of the direct conversion receiver. These are produced with large off-chip capacitors. The Baseband filter consists of two stages, DTOS and BIQUAD. The DTOS is a differential to single-ended converter having 8dB or 18dB gain. The BIQUAD is modified Sallen-Key Biquad.

Integrated resistors and capacitors are tunable. These are controlled with a digital control word via Hagar serial interface. The correct control words that compensate for the process variations of integrated resistors and capacitors and of tolerance of off chip capacitors are found during RX filter calibration.

Next stage in the receiver chain is the AGC-amplifier, also integrated into HAGAR. The AGC has digital gain control via serial mode bus from COBBA IC. The AGC-stage provides gain control range (40 dB, 10 dB steps) for the receiver and also the necessary DC compensation. One 10 dB AGC step is implemented in DTOS stages.

DC compensation is made during DCN1 and DCN2 operations (controlled via serial bus). DCN1 is carried out by charging the large external capacitors in the AGC stages to a voltage which cause a zero dc-offset. DCN2 set the signal offset to constant value (VREF RX 1.2 V). The VREF RX signal (from COBBA GJP) is used as a zero level to RX ADCs.

Single ended filtered I/Q-signal is then fed to ADCs in COBBA-IC. Input level for ADC is 1.4 Vpp max.

Transmitter

Transmitter chain consists of final frequency IQ-modulator, dualband power amplifier and a power control loop.

I- and Q-signals are generated by baseband also in COBBA-ASIC. After post filtering (RC-network) they go into IQ-modulator in HAGAR. LO-signal for modulator is generated by VCO and is divided by 2 or by 4 depending on system mode, EGSM/DCS1800. After modulator the TX-signal is amplified and buffered. There are separate outputs for both EGSM and DCS1800. HAGAR TX output level is 5 dBm.

Next TX signals are converted to single ended by baluns. Then TX signals are amplified and buffered in discrete buffers. In EGSM branch there is a SAW filter after the balun to attenuate unwanted signals and wideband noise from the Hagar IC.

The final amplification is realized with dualband power amplifier. It has one 50 ohm input and two 50 ohm outputs. There is also a gain control, which is controlled with a power control loop in HAGAR. PA is able to produce over 2 W (3 dBm input level) in EGSM band and over 1 W (6 dBm input level) in DCS1800 band into 50 ohm output. Gain control range is over 35 dB to get desired power levels and power ramping up and down.

Harmonics generated by the nonlinear PA are filtered out with the diplexer inside the RX/TX switch-module.

Power control circuit consists of discrete power detector (common for EGSM and DCS1800) and error amplifier in HAGAR. There is a directional coupler connected between PA output and RX/TX switch. It is a dualband type and has input and outputs for both systems. Dir. coupler takes a sample from the forward going power with certain ratio. This signal is rectified in a schottky-diode and it produces a DC-signal after filtering.

This detected voltage is compared in the error-amplifier in HAGAR to TXC-voltage, which is generated by DA-converter in COBBA. TXC has got a raised cosine form ($\cos^4$ - function), which reduces switching transients, when pulsing power up and down. Because dynamic range of the detector is not wide enough to control the power (actually RF output voltage) over the whole range, there is a control named TXP to work under detected levels. Burst is enabled and set to rise with TXP until the output level is high enough, that feedback loop works. Loop controls the output via the control pin in PA to the desired output level and burst has got the waveform of TXC-ramps. Because feedback loops could be unstable, this loop is compensated with a dominating pole. This pole decreases gain on higher frequencies to get phase margins high enough. Power control loop in HAGAR has two outputs, one for each freq. band.

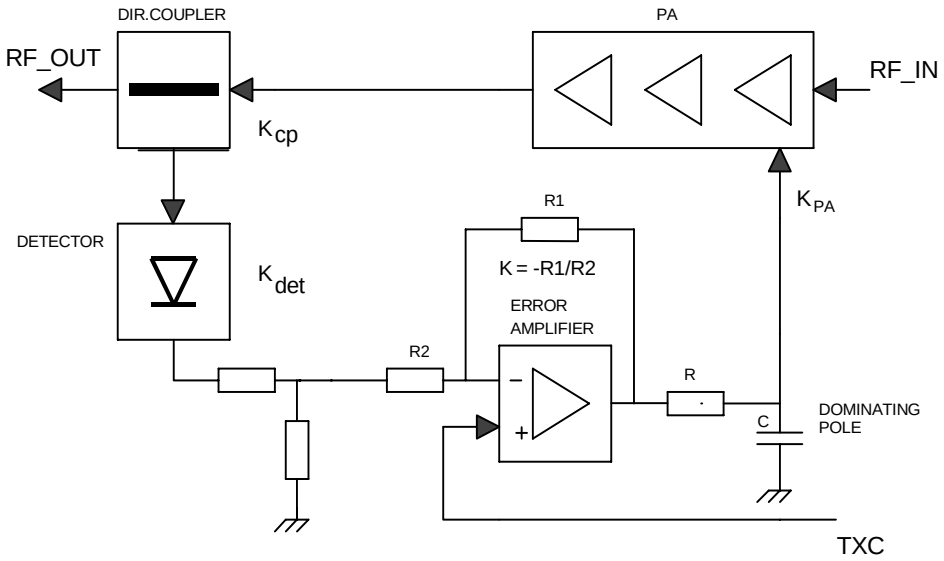


Figure 21: Transmitter

AGC strategy

AGC-amplifier is used to maintain output level of the receiver in certain range. AGC has to be set before each received burst, to do this pre-monitoring is used to give an estimate of the signal level.

There is 50 dB accurate gain control (10 dB steps) and one larger step (~30 dB) in LNA. LNA AGC step size depends on channel with some amount.

RSSI must be measured accurately on range -48...-110 dBm. At levels higher than -48 dBm the RX level reported by the MS to the base station is always 63.

Production calibration is done with two RF-levels, the LNA gain step is not calibrated.

AFC function

AFC is used to lock the transceiver frequency to the frequency of the base station. AFC-voltage is generated in COBBA with 11 bit DA-converter. There is a RC-filter in AFC control line to reduce the noise from the converter. Settling time requirement for the RC-network comes from signaling, how often PSW (pure sine wave) slots occur. They are repeated after 10 frames, meaning that there is PSW in every 46 ms. AFC tracks base station frequency continuously, so transceiver has got a stable frequency, because changes in VCTCXO-output don't occur so fast (temperature).

Settling time requirement comes also from the start up-time allowed. When transceiver is in sleep mode and "wakes" up to receive mode, there is only about 5 ms for the AFC-voltage to settle. When the first burst comes in system clock has to be settled into +/- 0.1 ppm frequency accuracy. The VCTCXO-module requires also 5 ms to settle into final frequency. Amplitude rises into full swing in 1...2 ms, but frequency settling time is higher so this oscillator must be powered up early enough.

DC-compensation

DC compensation is made during DCN1 and DCN2 operations (controlled via serial bus). DCN1 is carried out by charging the large external capacitors in AGC stages to a voltage which cause a zero dc-offset. DCN2 set the signal offset to constant value (VREF RX 1.2 V).Receiver Characteristics.

Receiver Characteristics

Table 18: Receiver Characteristics

Item	Values
Type	Direct conversion, Linear, DualBand, FDMA/TDMA
LO frequencies	3700 ... 3840 MHz / 3610 ... 3760 MHz
Typical 3 dB bandwidth	+/- 104 kHz
Sensitivity	min. - 102 / - 102 dBm (EGSM/PCN) , S/N >8 dB
Total typical receiver voltage gain (from antenna to RX ADC)	90 dB
Receiver output level (RF level -95 dBm)	350 mVpp , single ended I/Q-signals to RX ADCs
Typical AGC dynamic range	80 dB
Accurate AGC control range	50 dB
Typical AGC step in LNA	30 dB
Usable input dynamic range	-102 ... -10 dBm
RSSI dynamic range	-110 ... -48 dBm
Compensated gain variation in receiving band	+/- 1.0 dB

Transmitter Characteristics

Table 19: Transmitter Characteristics

Item	Values
Type	Direct conversion, dualband, non-linear, FDMA/TDMA
LO frequency range	3520 ... 3660 / 3420 ... 3570 MHz
Output power	2 W / 1 W peak
Gain control range	min. 30 dB
Maximum phase error (RMS/peak)	max 5 deg./20 deg. Peak

User Interface

The following circuits belongs to UI:

- LCD Module

- Keyboard

- Backlight circuit (for Keyboard and Display)

- Power key

- UI-Switch

LCD Module

The display circuit includes LCD module GD47 (84x48 pixels) and 2 capacitors. The LCD module is COG (Chip on Glass) technology. The connection method for chip on the glass is ACF, Adhesive Conductive Film. The LCD module is connected to the PCB with spring contacts. Capacitors are placed on PCB.

The display driver includes HW-reset, voltage tripler or quadrupler which depends on temperature, temperature compensating circuit and low power control. Driver includes 84x48 bit RAM memory that is used when some elements are created on display. Elements are created by software. Driver doesn't include CG-ROM. One bit in RAM is same as one pixel on display.

HW Interface is only for DCT3 Display.

Keyboard

HDa12 has 16 keys and uses 4 rows and 5 columns. Scanning is used for keyboard reading. Rows and columns are connected to MAD2WD1 interface.

The 'Key-domes', which are connected to the ROW-signals from the MAD, are sensible to ESD and are protected by an ESD network (ESDA6V1W5). In addition, serial resistors of 1K are inserted between the Keyboard Rows and the MAD.

	COL 0	**COL 1**	**COL 2**	**COL 3**	**COL 4**
ROW 0					
ROW 1	Up/Soft C	Down/Red			3
ROW 2	0	1	6	9	#
ROW 3	Down 2	2	5	8	Soft-A/Up 2
ROW 4	Clear/Soft B	Green	4	7	*
ROW 5					

Shaded areas - not used

Power Key

Power key is connected between GND and CCONT-pin 'PWRONX/ WDDISX'. Power key is active in LOW State and connected to ROW1.

Backlight for Display and Keyboard

Display Backlight is made by 4 LEDs connected in parallel (in bottom of the Display).

Keyboard Backlight is made by 4 LEDs connected in parallel.

Color of all LEDs is yellow-green, l = 570nm

Switching circuits for Display and keyboard backlight is controlled separately by the following signals:

KBLIGHTS:

KBLIGHTS-signal = HIGH -> the lights are on.

KBLIGHTS-signal = LOW -> the lights are off.

LCDLIGHTS:

LCDLIGHTS-signal = HIGH -> the lights are on.

LCDLIGHTS-signal = LOW -> the lights are off.

UISWITCH is used for controlling backlight.

UI-Switch

Detailed description of the UISWITCH is given in document /16/.

The UISWITCH is an integrated switch IC for UI (user interface) purposes. It includes control switch for buzzer and vibra, LED-control (display & keyboard) and two current sinks for LED's.

Features:

- 2 adjustable constant current sink (60mA each) for keyboard and LCD-LEDs
- LED ON/OFF control (separated for keyboard and LCD)
- Buzzer ON/OFF control
- FET switch (low Rds-on) for buzzer current
- Vibra ON/OFF control
- FET switch for vibra current
- Thermal shutdown
- Power down function for optimum current consumption
- Package TSSOP20 because of 1.5mm height requirement

Audio and Vibrator

Audio parts and vibrator is implemented on the same PCB board as BB-module and RF-module.

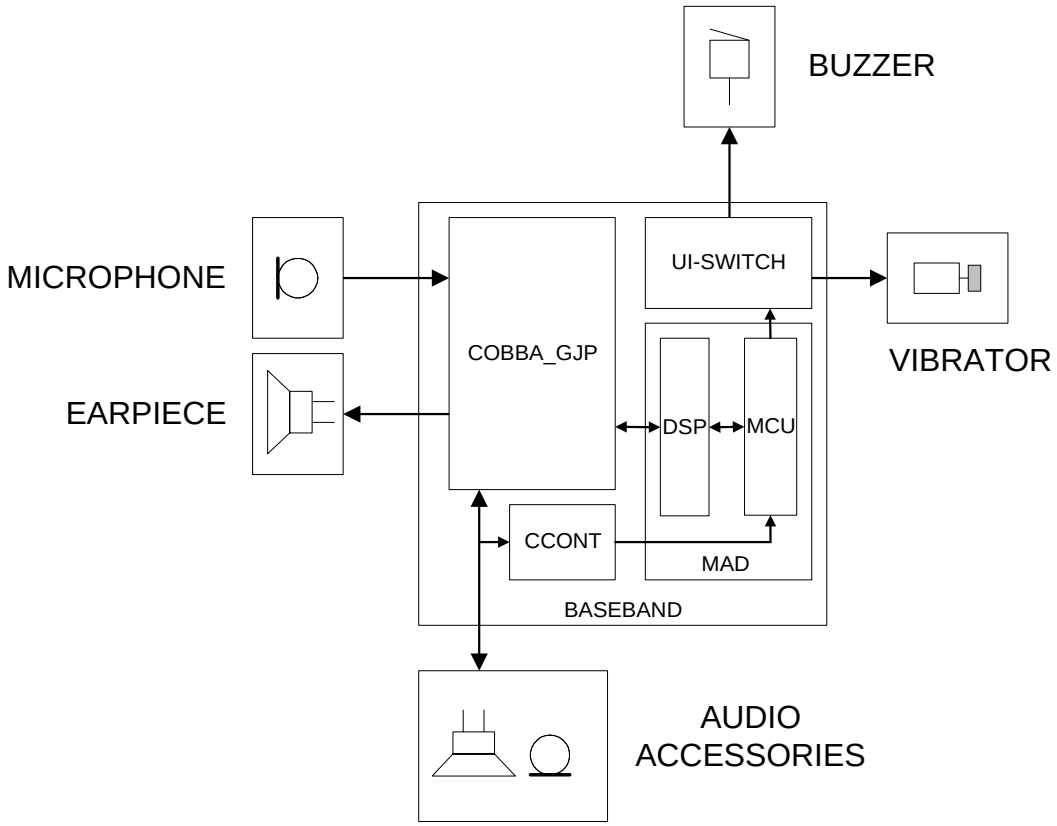


Figure 22: Audio /Vibrator Schematic

Audio Function Description

Audio control

The audio control and processing are taken care by the COBBA-GJP, which contains the audio (and RF) codec; and MAD2. MAD2 contains MCU and DSP blocks, handling and processing the audio signals.

The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or a handsfree-unit (PPH-1) microphone. The microphone signals from different sources are connected to separate inputs at the COBBA-GJP ASIC. Inputs for the microphone signals are differential type.

MIC1 input is used for the microphone output of a handsfree unit. The internal microphone is connected to the MIC2 input, and the MIC3 is used for the headset.

In COBBA there are also three audio signal outputs of which the dual ended (and not differential!) EAR lines are used for internal earpiece and HF lines for accessory audio output. The third audio output, AUXOUT, is used for bias supply to the headset microphone.

Input and output selection and gain control is performed inside the COBBA-GJP ASIC according to control messages from the MAD2. DTMF and other audio tones are generated and encoded by the MAD2 and transmitted to the COBBA-GJP for decoding.

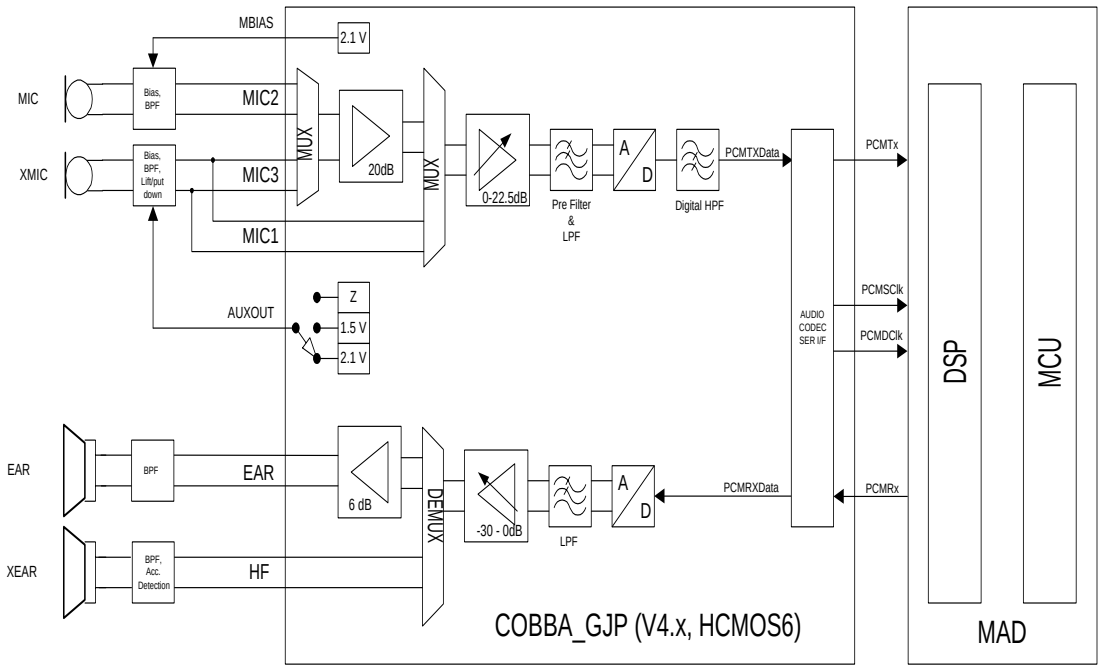


Figure 23: Audio Block Diagram (version 4)

Internal Audio Devices

HDa12's audio design is described in the following sections.

Ear Piece

Earpiece solution is selected to be PSS[)] earpiece. Earpiece design is leak tolerant. Design of the earpiece has been limited by HDa52/62/72, since all projects had to use the same A-cover. A common solution has been found, which can be used by all projects. It has resulted in some compromises.

The earpiece is designed to be approved by type 3.2, low leak artificial ear (Ear Simulator Type 4195, Low Leakage). It should also be possible to approve the earpiece design by type 1 artificial ear (Ear Simulator Type 4185), because of the American marked.

Earpiece Electric Interface

The low impedance, dynamic type earphone is connected to the differential output (EAR) in the COBBA, the audio CODEC.

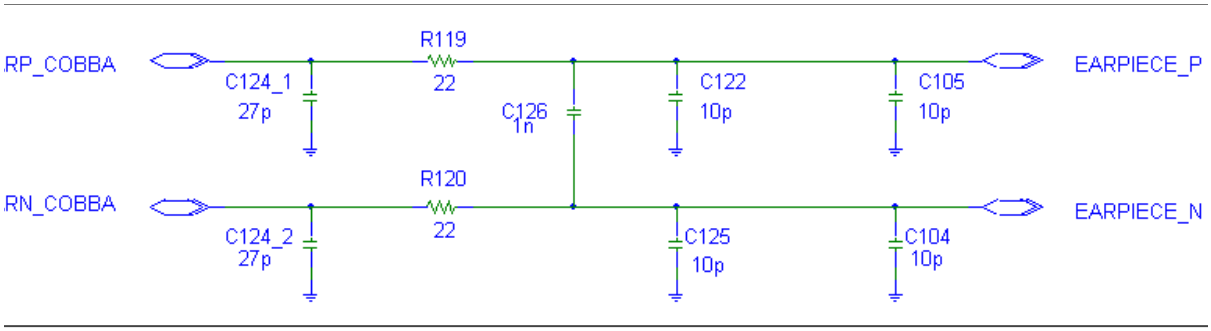


Figure 24: Internal Ear Piece Electric Interface

Microphone

An omni directional microphone is used . The microphone is placed in the system connector sealed in its rubber gasket. The sound port is provided in the system connector.

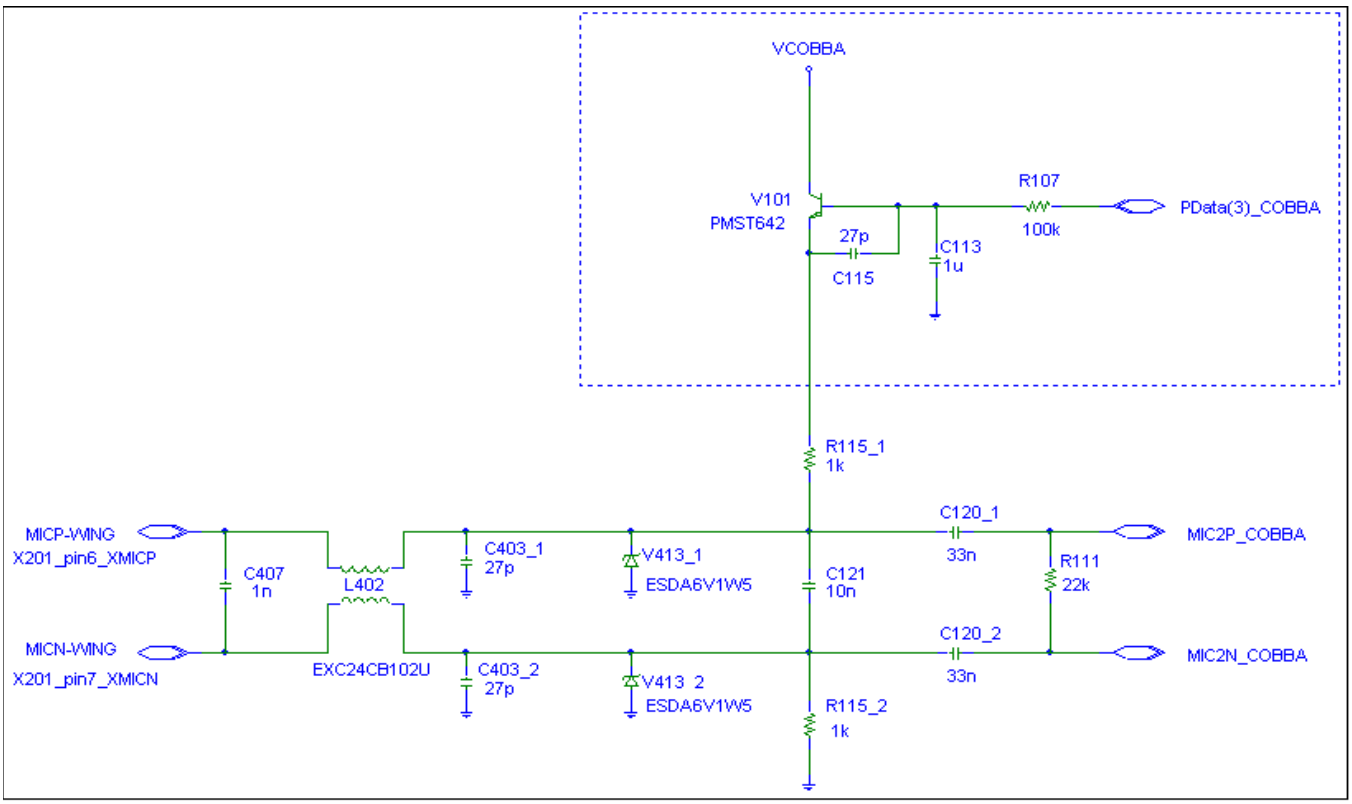


Figure 25: Internal Microphone Electrical Interface

Buzzer

Alerting tones and/or melodies are generated by a buzzer, which is controlled by a PWM signal from the MAD via an UI-SWITCH. The SPL requirement is 102dB (A) at 5cm. (Marketing target 105dB(A))

Buzzer is designed to be placed on the D-cover and fastened to it by two wings. The sound holes are placed in the A-cover.

The buzzer is lifted up from the PCB to find extra room on the PCB for the other BB components. The buzzer is electrically connected to the PCB by spring contacts.

Buzzer Electric Interface

The electric interface is shown below and the tables that follow show the relevant electrical specificions.

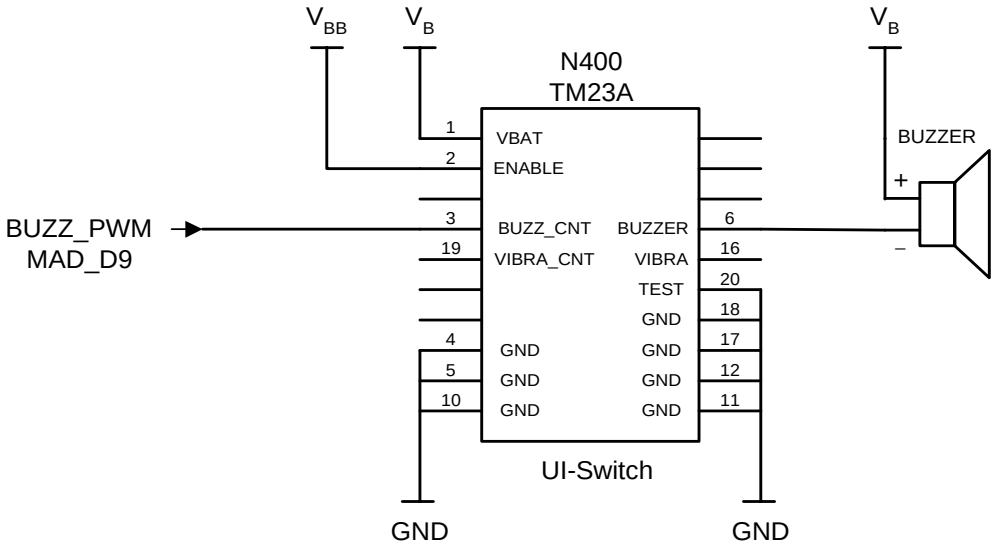


Figure 26: Buzzer Electrical Interface

Table 20: Interface-MAD and UI Switch

Signal	Parameter	Min	Typ	Max	Unit
BUZZ_PWM Buzzer Control Signal From the MAD	PWM low level, logic low	0	0.2	0.5	V
	PWM high level, logic high	2.0	2.5	2.9	V
	Current MAD output			2	mA
	Buzzer PWM frequency	100		10000	Hz
	PWM duty cycle (256 linear steps)	0		100	%
BUZZ_CNT Buzzer Control Signal in the UI-Switch	PWM low level, logic low	0		0.5	V
	PWM high level, logic high	2.00	2.80	2.85	V
	Internal Pulldown Resistor	60	100	180	kΩ

Table 21: Interface -Ui Switch and buzzer

Signal	Parameter	Min	Typ	Max	Unit	Notes
VBAT	Supply Voltage	3	3.6	5.2	V	
GND	Ground		0		V	
BUZZER	Buzzer Average Current			90	mA	50%dc@3.6v

Audio Accessories

HDa12 HP has the external audio interface to support the following Janette accessories:

HDC-5 : Headset with button

Headset is the most simple audio accessory to use. It merely only consists of an earpiece and a microphone, and a switch which in technical terms is often referred to as a HOOK-switch or HeadSet button. The HOOK-switch can be used either to answer in-coming calls or to end a call.

HDC-5 is purely a **passive audio accessory**.

PPH-1 : Plug & Play unit (carkit-unit)

Plug & Play HandsFree is an **active audio accessory** meant to be supplied from the cigaretlighter in a car. Plug & Play HandsFree contains an integrated loudspeaker and an option to connect an external microphone unless the phone's own microphone shall be used. The term 'Plug & Play' refers to the fact that the PPH-1 unit can be moved around in different cars.

HFM-8 : External microphone

HFM-8 is an option for the user to have a separate microphone for the carkit-installation. HFM-8 is supposed to be connected to PPH-1 which will then provide amplification of the uplink audio signal for the phone. HFM-8 is meant to be permanently installed in a car.

LPS-3: Loopset

Is detected and handled as the HDC-5. A current loopset, driven by a current amplifier, is used here instead of the earpiece.

External Audio Interrface

The interface is basically a 4-wire solution which gives two completely separate audio-paths, microphone- and earpiece-signals.

The interface is split up into :

External earpiece / speaker : **XEARP** (external earpiece, positive)

XEARN (external earpiece, negative)

External microphone : **XMICP** (external microphone, positive)

XMICN (external microphone, negative)

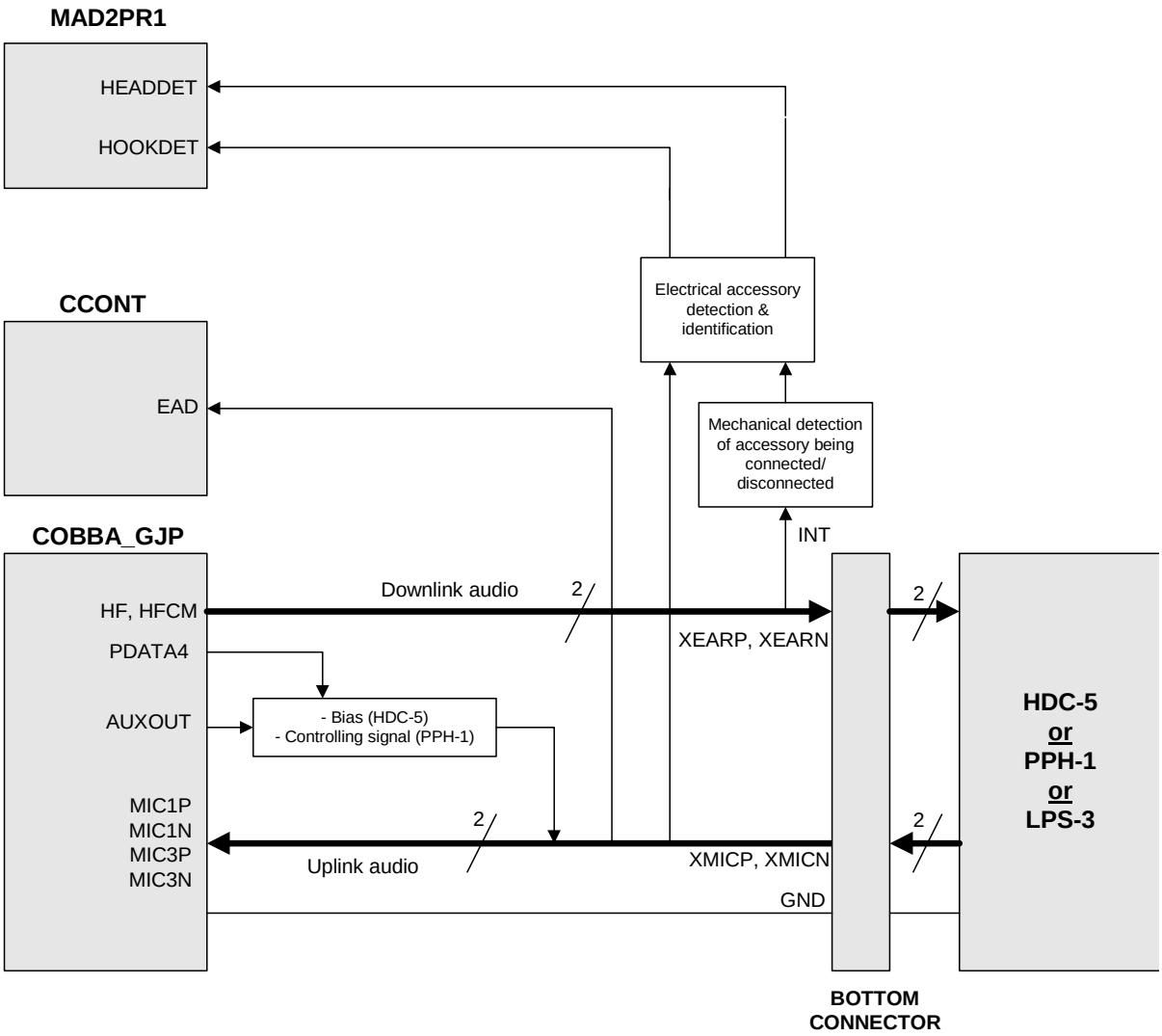


Figure 27: External Audio Interface- Block Diagram

Compared to DCT3 the Janette interface doesn't include a digital audio interface. The audio is only analogue.

External Audio Interface — Electrical Interface

The external audio connections are presented in the following two diagrams. A headset or a handsfree can be connected directly to the system connector. The headset microphone bias is supplied from COBBA AUXOUT output and fed to the microphone through XMICP line.

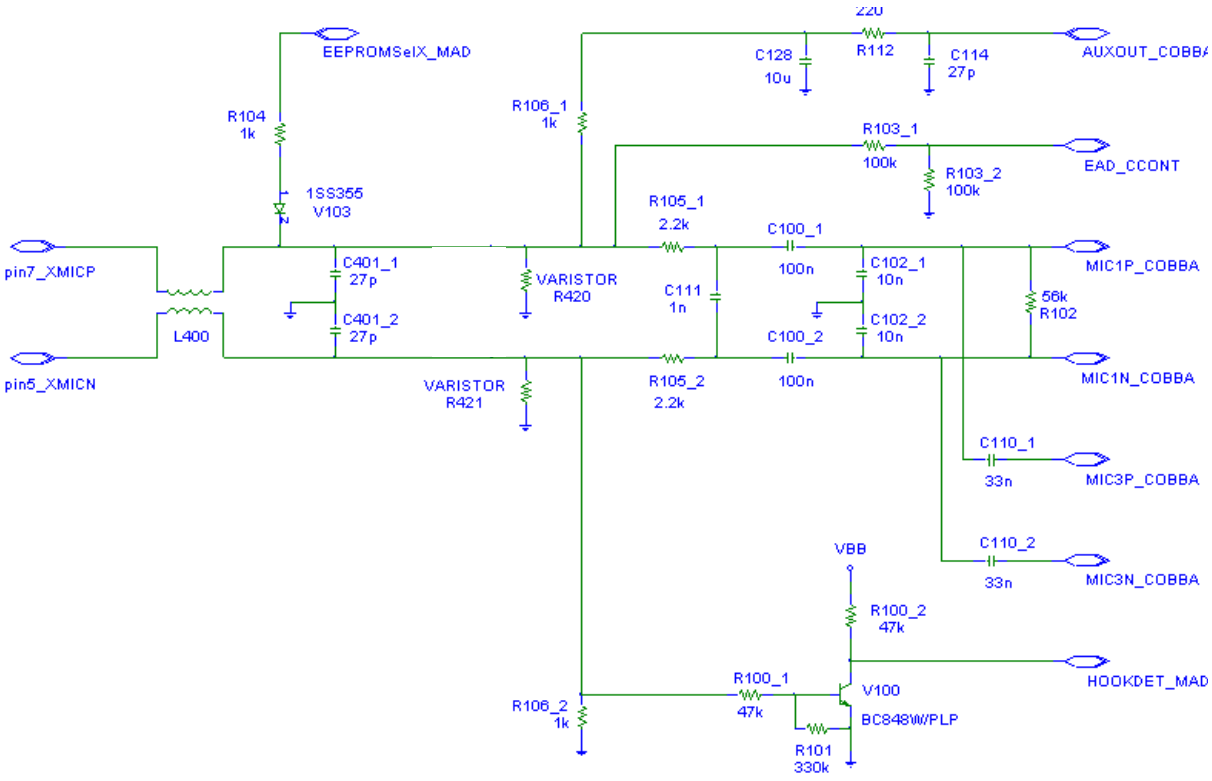


Figure 28: External Audio Interface - Microphone

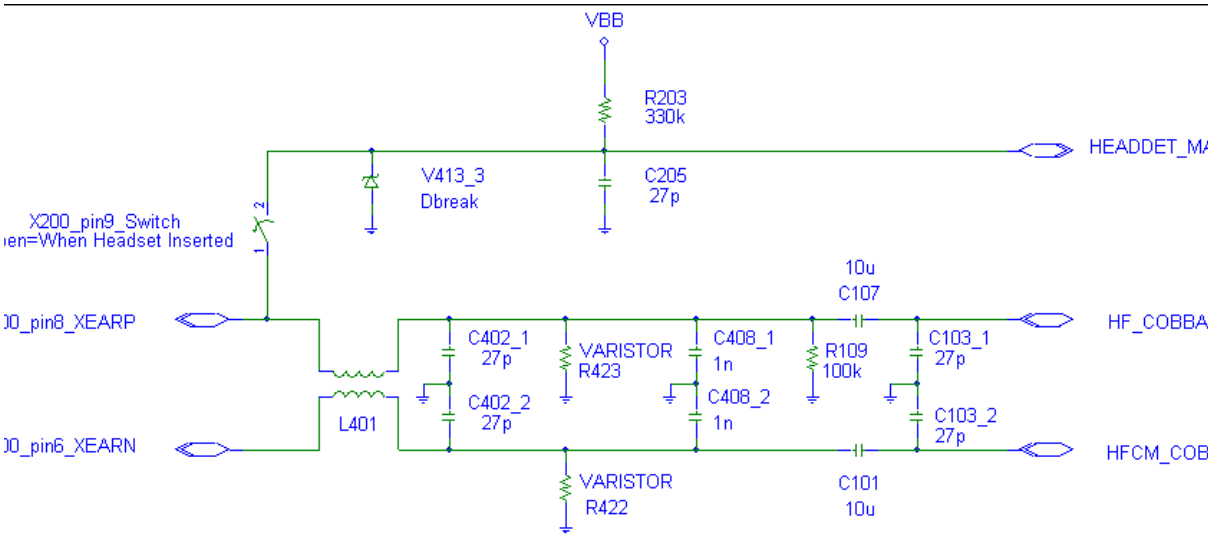


Figure 29: External Audio Interface - Speaker

HEADDET and **HOOKDET** are both the same type of 'interrupts input' in MAD.

The characteristic for these interrupts is shown in Triggering levels/Forbidden Operating Range-HEADDET and HOOKDET.

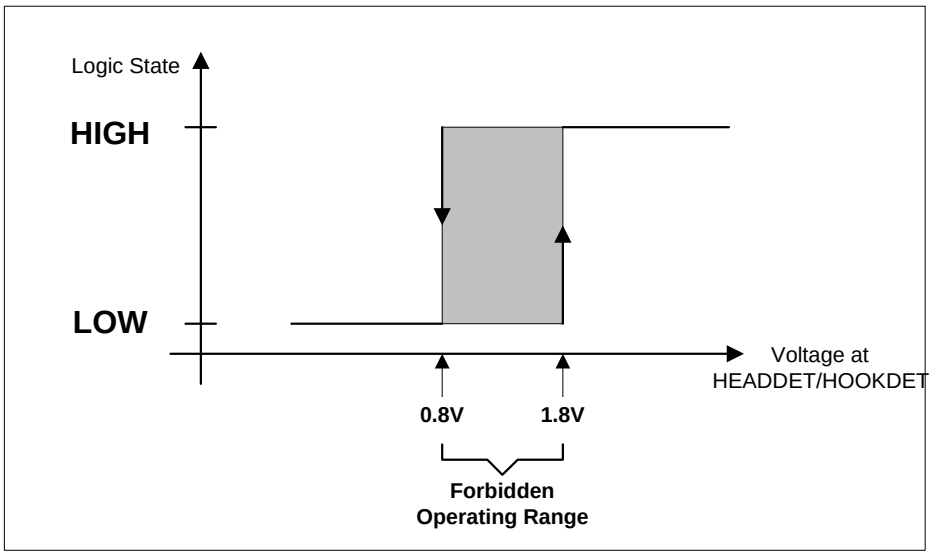


Figure 30: Triggering levels/Forbidden Operating Range-HEADDET and HOOKDET

If operating outside the ranges 0-0.8 V_{DC} or 1.8-2.8V_{DC} the interrupt inputs will start pulling current.

EAD is an analogue input on CCONT used to measure the DC-voltage on MIC1P line. This voltage value is used to identify the accessories and to control their function.

HF and **HFCM** are two audiooutputs through which audio can be routed to either HS-earpiece or PPH-1 speaker. HF and HFCM are externally wired as fully- differential outputs, however it is only HF which in reality performs the audio-amplification.

MIC1P, MIC1N, MIC3P and **MIC3N** are all inputs to the microphone amplifier in COBBA. In short form the main difference for the listed inputs are :

MIC1P, MIC1N : Rated to audiosignals up to 2 Vpp. Used for PPH-1 microphone.

MIC3P, MIC3N : Rated to audiosignals up to 200 mVpp. Used for HS microphone.

Both types of inputs can be wired and used to either fully differentiel or singled-ended operation, however the fully differential configuration is chosen for the Janette interface.

MIC1 and MIC3 must be isolated from each other DC-wise !

AUXOUT is an output having two functions in the Janette Accessory interface:

Biasing purposes for the HeadSet-microphone

Controlling purposes for the PPH-1. AUXOUT can be set to the following states by the MCU-SW :

High Impedance (Z)

2.1 Vdc

1.5 Vdc

Low Impedance (0 Vdc)

External Audio Connector

The accessibility to the external audio interface is reached by the system connector, containing a 4-pole Jack plug. The Jack plug which is integrated in the system connector contains a mechanical switch which is used to detect the connection of the accessories.

The configuration for the 4-pole Jack-plug is shown in the following figure.

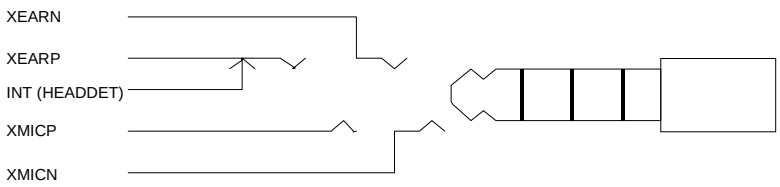


Figure 31: 4 Pole Jack plug for audio accessories

External Audio Signal Electrical Specifications

Table 22: External AudioSignals - Electrical Specifications

Name	Min	Typ	Max	Unit	Notes
XMICP & XMICN		2.2		kΩ	Input AC impedance
			1	Vpp	Maximum signal level
		2.1		V	Output DC level
			500	µA	Bias current
XEARP & XEARN		47		W	Output AC impedance (ref. GND)
		10		µF	Series output capacitance (ref. GND)
	1.18	1.25		Vpp	Output Swing♠)
		2.8		V	DC voltage (330k pull-up to VBB) (When acc. is not connected!)

Table 22: External AudioSignals - Electrical Specifications

Name	Min	Typ	Max	Unit	Notes
HEADDET			9.15	uA	When accessory is not connected.
VIN	0		12	V	Charger Input Voltage
GND	0		0.3	V	Ground

♠) Ouput swing @ 0dBm0, GR = -6dB. 0dBm0 means input amplitude into receive path at 3.14 dB below overload point. Overload point would correspond to 1.80 V_{PP}. The output is referenced around the common DC output voltage, 1.35V. Ref. GND.

Accessory Detection, Identification and Control

Accessory Detection

XEARP signal has a 300k pullup (R203) and 100k pulldown resistor (R109). By these the HEADDET is pulled up when **an accessory is connected**, and pulled down when **disconnected**. See Figure 29, "External Audio Interface - Speaker," on page 55 . (The system connector must be assembled otherwise the transceiver will assume that some accessory is connected!)

HOOKDET and HEADDET Truth Table

Accessory connected	HeadDet	Notes
No accessory connected	Low	-
An accessory connected	High	XEAR and XMIC loaded (dc)

Accessory Identification

The voltage level on XMICP signal is measured by CCONT at its ADC input, EAD. This voltage level is used to determine the **type of accessory**. For details see DOC. DHJ00143-EN, HD947/Basic implementation of Janette accessory interface.

Accessory Control

Headset

In the HDC-5 the HeadSet-button is electrically connected across the XMICP and XMICN lines) . When the HeadSet button is activated, a change in the current through the microphone's bias resistors appears. Based on this change, a transistor-switch (V100) controls the logic state of the HOOKDET in the MAD (See Figure 28, "External Audio Interface - Microphone," on page 55). When the switch on the headset is pressed, the switch (V100) goes on and the HOOKDET will go to the low level state. This is used **to lift the receiver or to put it down.**

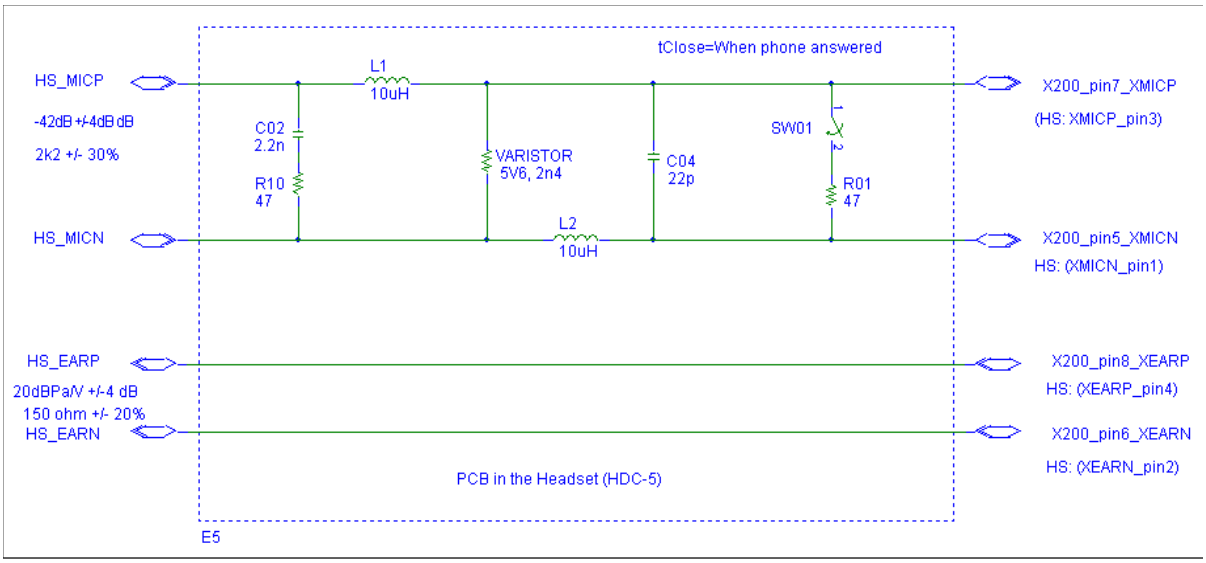


Figure 32: HDC-5 Schematic

(The voltage value at EAD input is used to control if the Headset remains connected. The voltage at EAD can also be used to detect a keypress, but it can fails, if the key is pressed with a low interva

Detection of Handset keypress

	HS button	HOOKDET	EAD
AUXOUT = 'Z' (HS Connected)	Open	H	-
	Closed	H	-
AUXOUT = 2.1Vdc (HS Connected)	Open	H	≈ 750 - 1050 mVdc
	Closed	L	≈ 600 - 700 mVdc

Accessories Electric Specifications

Table 23: HDC-5 Electrical Specifications

	Min	Typ	Max	Comment
Impedance, Transmitting	1540 Ω	2200 Ω	2860 Ω	
MIC Bias		2.1 V		
HDC-5 microphone current			400 µA	
Impedance, Receiving	112 Ω	150 Ω	188 Ω	
HDC-5 button closed resistor		2 × 22 Ω		± 5 %

(Experiences have shown that a decrease of HS-mic current from 500 µµA to 400 µµA is needed in order to have safe margins.)

Table 24: PPH-1 Electrical Specifications

	Min	Typ	Max	Comment
XMICP		60 mV RMS	350 mV RMS	Signal Level
			1 V_{PP}	Max. Signal Level
		100 Ω		Accessory Source Impedance
	2.095 V_{DC}	2.182 V_{DC}	2.269 V_{DC}	Wxternal mic. detection.
	2.519 V_{DC}	2.603 V_{DC}	2.687 V_{DC}	Internal mic. detection.
	1. 840 V_{DC}			Accesoty muted.
XMICN		60 mV RMS	350 mV RMS	Signal level.
			1 V_{PP}	Max. signal level.
		100 Ω		Accessory Source Impedance.
XEARP		60 mV RMS	300 mV RMS	Signal level.
		47 Ω		Output AC Impedance.
			850 mV_{PP}	Max output level.
		6.8 kΩ		Resistance to XEARN
XEARN		60 mV RMS	300 mV RMS	Signal level.
		47 Ω		Output AC Impedance.
			850 mV_{PP}	Max output level.
		6.8 kΩ		Resistance to XEARP
GND	-0.4 VDC	-0.2 VDC	0 VDC	VDC compared to phone GND.
		600 mADC	750 mADC	
V_CHARGER			8 VDC	Charging voltage.
		600 mADC	750 mADC	Charging current.
			100 mV_{PP}	Ripple f = 20-200 Hz.
			20 mV_{PP}	Ripple f = 0.2-30 kHz.
			100 mV_{PP}	Ripple f > 30 kHz.
			200 mV_{PP}	Total ripple f > 20 Hz.

Vibra Alerting Device

A vibra alerting device is used to generate a vibration signal for an incoming call. Vibra is located in the phone. The vibra is controlled by a PWM signal from the MAD and via the UI-SWITCH.

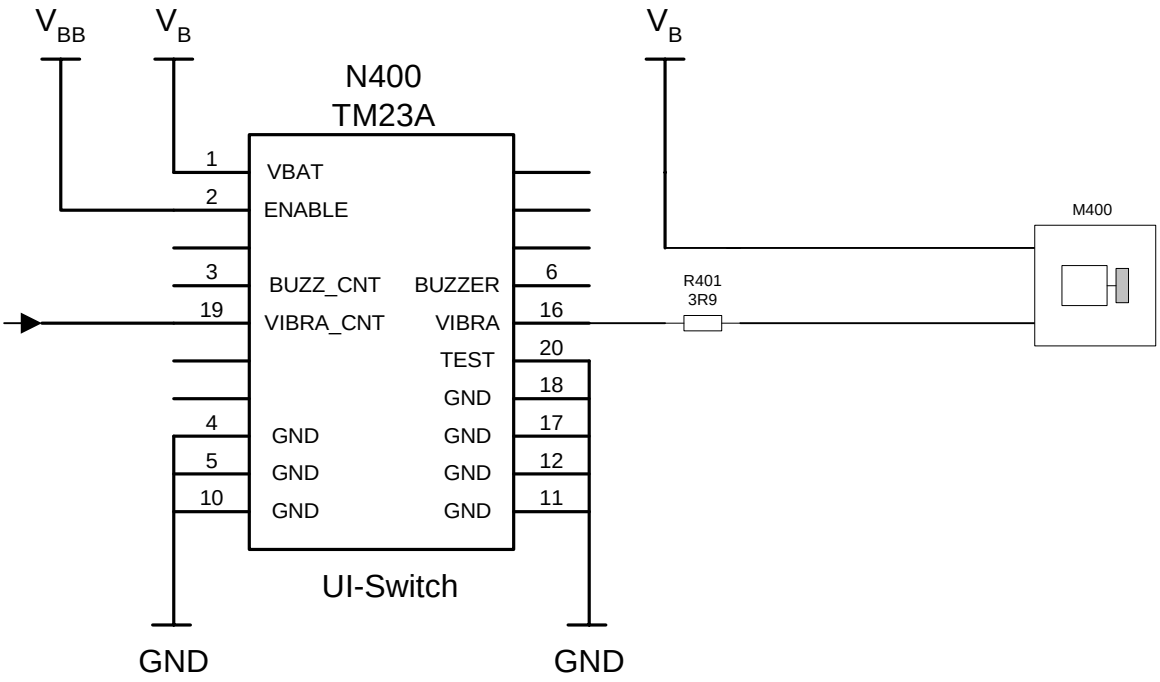


Figure 33: Vibrator Electrical Interface

Table 25: Interface -MAD UI Switch

Signal	Parameter	Min	Typ	Max	Unit	Notes
VIBRA_PWM Vibra Control Signal From MAD	PWM low level, logic low	0	0.2	0.5	V	
	PWM high level, logic high	2.0	2.5	2.9	V	
	Current MAD output			2	mA	
	Vibra PWM frequency		22k		Hz	
	PWM duty cycle (256 linear steps)	16		35	%	Theoretically!
VIBRA_CNT Vibra Control Signal in UI-Switch	PWM low level, logic low	0		0.5	V	
	PWM high level, logic high	2.00	2.80	2.85	V	
	Internal Pulldown Resistor	60	100	180	kΩ	

Table 26: Interface - UI Switch and Vibra

Signal	Parameter	Min	Typ	Max	Unit	Notes
VBAT	Supply Voltage	3	3.6	5.2	V	
GND	Ground		0		V	
VIBRA	Vibra Nominal Current		120		mA	3.6V@10Ω
	Vibra Start Current			175	mA	5.2V
	Vibra Peak Current			190	mA	5.2V
	Vibra Reverse Peak Current			340	mA	
	Vibra FET Switch R_{dson}			1	W	