AN691

Optimizing Digital Potentiometer Circuits to Reduce Absolute and Temperature Variations

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INTRODUCTION

Mechanical potentiometers are typically used to adjust system reference levels, gain errors and offset errors. Digital potentiometers can be used for the same functions while offering the added capability of digital adjustment control. Devices, such as Microchip's MCP41XXX and MCP42XXX digital potentiometer families, can be used much like a mechanical potentiometer in that they have three resistive terminals for the single versions (MCP41010, MCP41050, and MCP41100) and six resistive terminals for the dual versions (MCP42010, MCP42050, and MCP42100) as illustrated in Figure 1.

The two modes that a potentiometer can be configured in are the Rheostat mode and Voltage Divider mode. When used in the Rheostat mode, the wiper (terminal P_W), is shorted to either the P_A or P_B terminal of the device. This configuration is shown in Figure 2. When a digital potentiometer is used in the Voltage Divider mode (Figure 2.b) all three terminals are connected to differing nodes in the circuit.

In both of these configurations, the digital potentiometer will have a nominal resistance and temperature coefficient error that may affect the overall application unless precautions are taken. In this application note, circuit ideas will be presented that use the necessary design techniques to mitigate these errors, consequently optimizing the performance of the digital potentiometer.

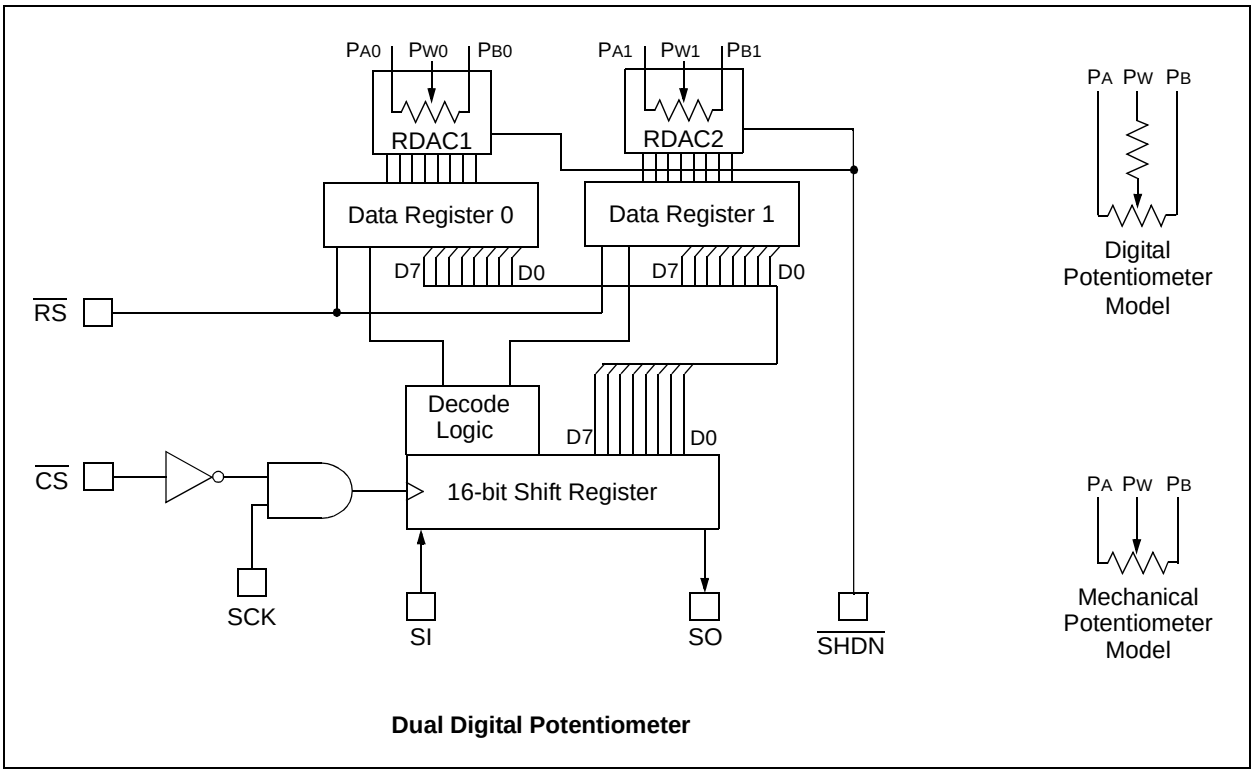


FIGURE 1: *The operation of the digital potentiometer as compared to the mechanical potentiometer is functionally the same. The adjustment of the digital potentiometer is done with a serial code to the device. Although the mechanical potentiometer provides simplicity, the digital potentiometer provides flexibility and reliability.*

Rheostat Mode Operation and Specifications

In the Rheostat mode, either terminal PA or PB are connected to the wiper terminal as shown in Figure 2.a. In this mode, the output resistance is digitally adjusted from the maximum nominal value, minus one LSB, down to zero ohms. The nominal resistance of the element in the Rheostat mode is calculated with the following formulas:

$$R_{BW} = \frac{R_{AB}(D_N)}{2^N} + R_W$$

or

$$R_{AW} = \frac{R_{AB}\left(2^N - D_N\right)}{2^N} + R_W$$

where:

RAW is the resistance between pin A and pin W of the digital potentiometer.

RAB is the nominal resistance across the entire potentiometer, from pin A to pin B.

RBW is the resistance between pin B and pin W of the digital potentiometer.

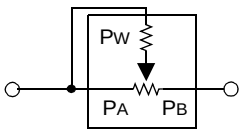
n is the number of digital potentiometer bits. For the MCP4XXXX family of potentiometers, the number of bits is eight.

Dn is the digital code in decimal form that is used to program the digital potentiometer. With the MCP4XXXX 8-bit digital potentiometers the programmable digital code ranges from 0 to 2^8 - 1 or 255.

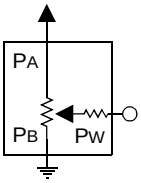
Rw is the parasitic resistance through the wiper.

As summarized in the table in Figure 2, the nominal resistance of the digital potentiometer varies, depending on the device selected. Additionally, the part to part variation of the nominal resistance is specified to be within a given percentage. For example, the nominal resistance of the MCP4X010 is 10 kΩ ±20%. The resistance variation of these digital potentiometers is primarily dependent on the process variation of the sheet-rho of a diffused p-silicon layer and the on-resistance of the internal switches.

The temperature variance of the digital potentiometers element is also shown in Figure 2. For instance, the variance of the MCP41010 (10 kΩ) digital potentiometer is 800 ppm/°C (typical). With this specification, the expected change of the total resistance of the MCP41010 is from 10 kΩ at 25°C to 9.52 kΩ at 85°C.



a. Rheostat Mode



b. Voltage Divider Mode

Device	Nominal RAB Resistance (typ)	RAB Change with Temperature (typ)	Nominal Resistance Match (typ)	RA, RB Relative Accuracy INL (typ)	Tempco Variance Between RA and RB (typ)	Code to Code Variance DNL (typ)
MCP41010 (single)	10 KΩ ±20%	800 ppm/°C	-----	±0.25 LSB	1%	±0.25 LSB
MCP42010 (dual)	10 KΩ ±20%	800 ppm/°C	0.2%	±0.25 LSB	1%	±0.25 LSB
MCP41050 (single)	50 KΩ ±30%	800 ppm/°C	-----	±0.25 LSB	1%	±0.25 LSB
MCP42050 (dual)	50 KΩ ±30%	800 ppm/°C	0.2%	±0.25 LSB	1%	±0.25 LSB
MCP41100 (single)	100 KΩ ±30%	800 ppm/°C	-----	±0.25 LSB	1%	±0.25 LSB
MCP42100 (dual)	100 KΩ ±30%	800 ppm/°C	0.2%	±0.25 LSB	1%	±0.25 LSB

FIGURE 2: *The resistive elements of the digital potentiometer can be configured in (a.) the Rheostat mode or (b.) the Voltage Divider mode. Each mode has its own set of performance specifications.*

Digital Potentiometer Circuits Configured in the Rheostat Mode

The level of nominal resistive matching that is shown in Figure 2 can be acceptable for some applications. However, if a degree of precision is desired, the dual potentiometer can be used to an advantage in the Rheostat mode. With the dual digital potentiometer, the nominal resistances between the two potentiometers are ratio matched to a very small percentage as shown in Figure 2. For instance, the matching of the two resistive potentiometer elements in the MCP42010 (dual, 10 kΩ) is guaranteed to be less than ±0.2% (typ). This close relationship between the two resistor arrays can be used to a distinct advantage.

One circuit that takes advantage of the relationship between the two potentiometers in the dual, MCP42100 is shown in Figure 3.

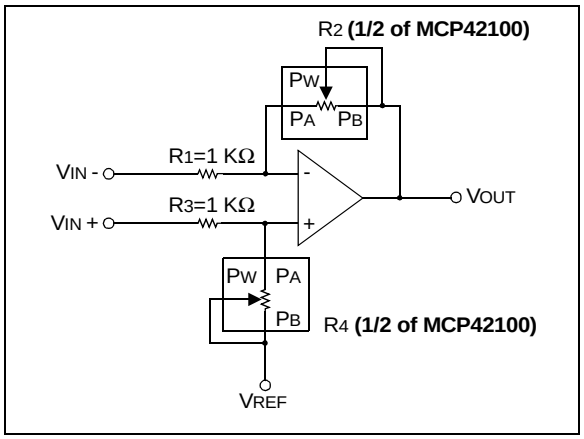


FIGURE 3: *The digital potentiometers in this differential amplifier can be programmed to change the gain of the circuit as well as enhance the common-mode rejection. The common-mode rejection of this circuit is fairly immune to temperature changes.*

In Figure 3, the arrangement of the resistors around an operational amplifier is called the difference amplifier or op amp subtractor. The DC transfer function of this circuit is equal to:

$$V_{OUT} = \frac{V_1 R_4 (R_1 + R_2)}{((R_3 + R_4) R_1)} - V_2 \left(\frac{R_2}{R_1}\right) + V_{REF} R_3 \frac{(R_1 + R_2)}{((R_3 + R_4) R_1)}$$

If R1/R2 is equal to R3/R4, the system gain of this circuit equals:

$$V_{OUT} = (V_1 - V_2)\left(\frac{R_2}{R_1}\right) + V_{REF}$$

The fact that R1/R2 is equal to R3/R4 simplifies the mathematics in this system considerably. Since the gain of both input signals are the same, the common-mode voltage (CMV) of the two signals is conveniently subtracted from the output results.

Ideally, CMV changes are rejected by this circuit. The calculated common-mode rejection (CMR) error that is attributed to resistor mismatches in this circuit is equal to:

$$CMR = 100 \frac{\left(1 + \frac{R_1}{R_2}\right)}{\%\ of\ mismatch\ error}$$

where (% of mismatch error) is the mismatch in the equation R1/R2 = R3/R4.

An example of the impact of this error is demonstrated with a 12-bit, 5V system, where the gain of the circuit is 100V/V, the common-mode voltage ranges 0 to 5V and the matching error is ±0.2%. Using the formula above, the contributed error of this type of common-mode excursion is equal to 0.2 mV. This voltage is five times less than 1 LSB.

Adjustable gain is easily implemented by making the discrete resistors equal (R1=R3) and changing both potentiometers together as desired. Although, any digital potentiometer can be used in the R2 and R4 position in this circuit, the higher the nominal value of the digital potentiometer, the wider the adjustable gain range will be.

In a single supply environment, a voltage reference is used to center the output signal between ground and the power supply. This voltage is represented in this circuit as VREF. The VREF circuit function can be implemented with a precision voltage reference or with an adjustable voltage reference circuit that uses a digital potentiometer as shown in Figures 5, 6 and 7. The adjustable voltage reference designs offer the flexibility of removing offset system errors.

An alternative to the circuit shown in Figure 3 is illustrated in Figure 4. In this circuit configuration, the differential inputs are high impedance and the output is differential. There are three resistors used in this circuit, two of which are 1/2 of a dual potentiometer.

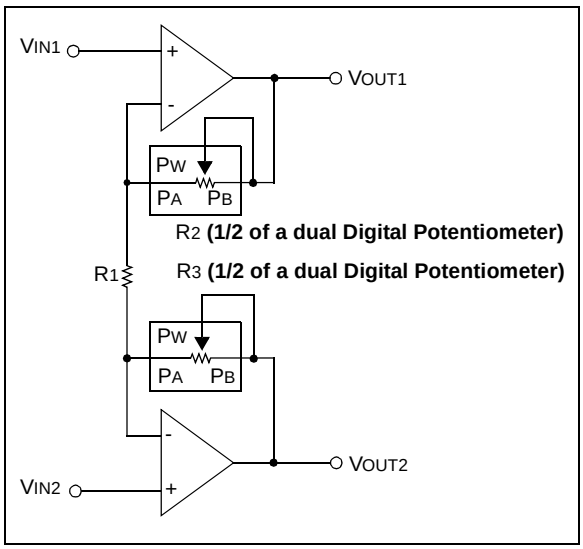


FIGURE 4: *This differential in and differential out circuit uses two digital potentiometers in the Rheostat mode. When the two digital potentiometers are set to be equal, the gains on the two input signals are equal.*

If $R_2 = R_3$, the transfer function of this circuit is:

$$(V_{OUT1} - V_{OUT2}) = (V_{IN1} - V_{IN2})\left(1 + \frac{2R_2}{R_1}\right)$$

This flexible gain circuit uses the matching of nominal resistance and thermal shifts of the dual potentiometer to an advantage.

Voltage Divider Mode: Operation and Specifications

In the Voltage Divider mode shown in Figure 2, all three terminals to the potentiometer are connected to separate nodes in the circuit. In this mode, the total resistance of the device is separated into two resistors. The first being the resistance from terminal PB to the wiper (PW) and the second is between terminal PA to the wiper. The relationship between these two resistors is equal to:

$$R_B = R_{AB}\frac{(D_n)}{2^n}$$

$$R_A = R_{AB}\frac{\left(2^n - D_n\right)}{2^n}$$

where:

RB is equal to the resistance between the PB terminal and PW terminal minus the wiper resistance.

RA is equal to the resistance between the PA terminal and PW terminal minus the wiper resistance.

There is a third resistance from the digital potentiometers element to the wiper terminal. This resistance is called the wiper resistance or RW. If the wiper of the digital potentiometer is followed by a high impedance node, errors caused by the wiper resistance are eliminated.

The absolute value of these resistances will still vary between ±20% and ±30% (depending on the device used), however as shown in the table in Figure 2, the ratio between the two elements will be much lower. In the case of the MCP4X010, the maximum mismatch error between RB and RA is ±0.098% (DNL specification).

The related temperature performance of these two resistors is also lower than the absolute temperature behavior at a typical 1 ppm/°C. Since the resistive elements of RB and RA are manufactured with the same material on the same chip, the ratio of the thermal changes with temperature is considerably better as compared to the single resistive element in the Rheostat mode.

Digital Potentiometer Circuits Configured in the Voltage Divider Mode

The digital potentiometer can be used very effectively in a variety of circuits when it is configured in the Voltage Divider mode. All of the following circuits take advantage of the resistive ratio matching of the two resistive elements (RB and RA).

Voltage Reference Circuits

One form of offset voltage adjustment is implemented with a voltage reference. This type of adjustment usually compensates for all of the system offset errors in the signal path.

In Figure 5, a digital potentiometer is used to design an adjustable voltage reference. In Figure 5.a, the potentiometer is placed between the positive power supply and ground. The output voltage of the adjustable reference is equal to:

$$V_{REF} = \frac{V_{DD}R_{POT-B}}{R_{POT-AB}}$$

The resolution of this reference circuit is dependent on the number of programmable bits of the digital potentiometer and the value of VDD. When using any of the 8-bit digital potentiometers from Microchip and a 5V supply, the nominal LSB size would be 19.53 mV.

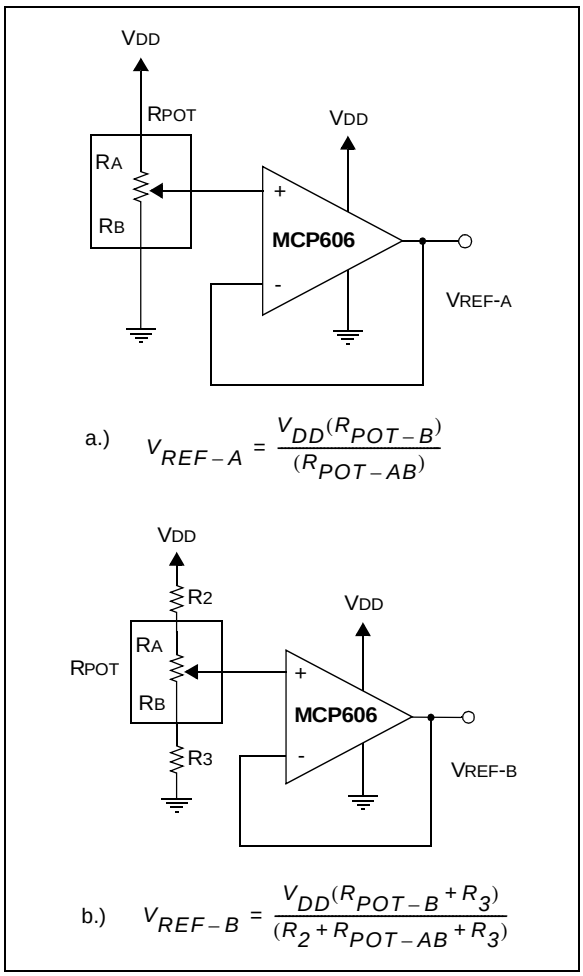


FIGURE 5: *A digitally adjustable reference can be designed using the power supply across the digital potentiometer (a). Higher accuracy can be achieved by using additional resistors (b) in series with the digital potentiometer.*

In this circuit, the operational amplifier acts to isolate or buffer the digital potentiometer resistance from following stages.

The absolute accuracy and over temperature performance of the voltage presented to the input of the amplifier is dependent on the matching of the digital potentiometer resistive elements as well as the stability of the power supply.

As an example of the effects of the digital potentiometer errors, the MCP4X010 (10 kΩ digital potentiometer) would perform with an absolute accuracy less than ±0.25 LSB (typ) or ±3.9065 mV at 25°C. Over temperature, the output voltage would typically vary 1% due to resistance matching. This translates into a typical variance over temperature (-40°C to +85°C) of 1.172 mV or ±0.585 mV. Adding this to the error at room temperature, the total possible error becomes ±4.99 mV. In this example, it is assumed that the power supply is a stable 5V.

If a smaller LSB size is required for an adjustable voltage reference that has the full dynamic range of the power supply voltage, the circuit in Figure 6 can be used.

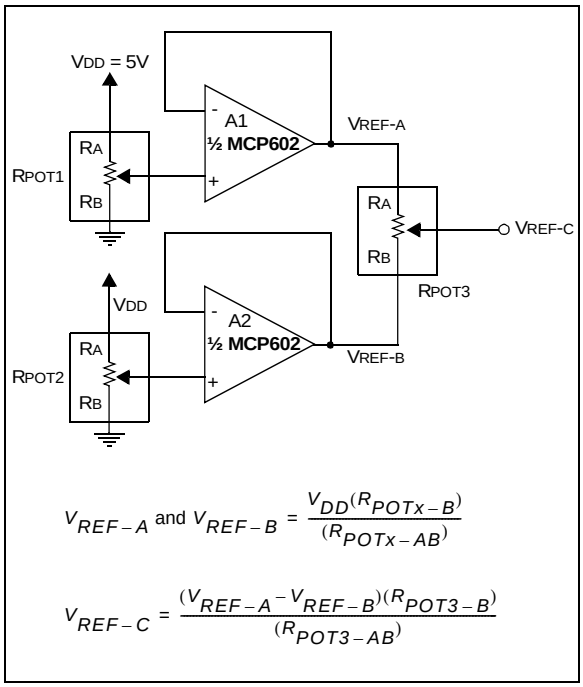


FIGURE 6: *Three digital potentiometers in combination with a dual amplifier can be configured for a wide dynamic range, adjustable voltage reference that has an ideal LSB size of $V_{DD}/2^{2n}$, where n is the number of digital potentiometer bits.*

In this circuit, the wiper voltage of R_{POT1} is buffered with A_1, a single supply, CMOS amplifier and R_{POT2} is buffered with A_2. The dynamic range of the output of A_1 and A_2 is equal to approximately (GND+50 mV) to (V_{DD}–1.2V). The positive output swing range is primarily restricted by the amplifiers maximum input common mode voltage. The theoretical LSB size of the voltages at V_{REF-A} and V_{REF-B} are equal to $V_{DD}/2^n$ or 19.53 mV.

The voltage difference of V_{REF-A} and V_{REF-B} is impressed across R_{POT3}. The difference of these voltages are then divided again by the third digital potentiometer to have an ideal LSB size equal to:

$$V_{REF-C} = \frac{(V_{DD}/2^n)}{2^n}$$

$$V_{REF-C} = \frac{V_{DD}}{2^{2n}}$$

The configuration in Figure 6 provides an theoretical output resolution of 16 bits. When V_{DD} is equal to 5V, the theoretical LSB size is 76.29 µV.

The value of the output of this precision adjustable reference is compromised by the absolute matching resistance and temperature coefficient of the digital potentiometers.

In the error analysis of this circuit, it can quickly be found that at 25°C, the nominal errors of the digital potentiometer have the highest potential to create the largest errors. This in shown in Table 1.

	Room Temp.	Over -40°C to 85°C range
R_{POT1} (±0.25 LSB typical error)	±0.019 mV	±0.003 mV
R_{POT2} (±0.25 LSB typical error)	±0.019 mV	±0.003 mV
R_{POT3} (±0.25 LSB typical error)	±0.019 mV	±0.003 mV
Total typical error at V_{REF-C}	±0.057 mV	±0.009 mV

TABLE 1: *This table shows the nominal and temperature errors effecting adjustable voltage reference shown in Figure 6. Calculations assume A_1 and A_2 are ideal amplifiers, the MCP4X010 digital potentiometers are used and V_{DD} = 5V. All values are referred to the output, V_{REF-C}.*

The errors of the first stage (including the amplifiers) are divided down by the second stage. Given this error analysis, the circuit in Figure 6 is accurate to 13.3 bits or ±0.057 mV. This analysis does not take into account variations in V_{DD} over temperature.

Another technique that can be used to design a precision adjustable voltage reference is shown in Figure 7.

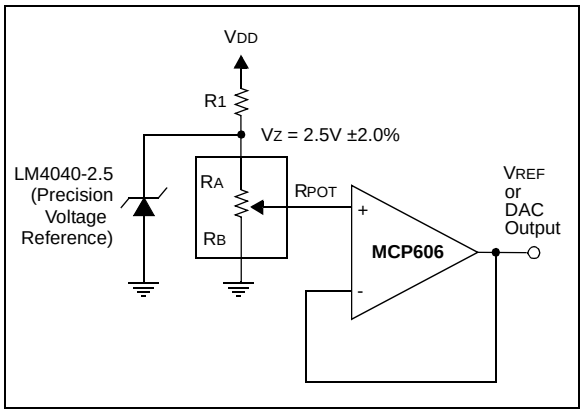


FIGURE 7: *A precision adjustable reference can be configured using a precision reference that is not adjustable along with a digital potentiometer. The value of R_1 is set so that the current through the LM4040 does not go below its minimum operating current.*

In this circuit, the variability of the power supply is stabilized with a precision voltage reference. Since the digital potentiometer is configured in the Voltage Divider mode, the errors at the output of the amplifier is similar to the errors discussed in Figure 5. The only difference being that the power supply is replaced with a precision reference. This configuration is often used when the digital potentiometer is used as a DAC.

Offset Adjustment Circuits

Offset adjustment can be implemented in the analog circuit by injecting a voltage into the signal path with a simple voltage divider or a complete adjustable voltage reference.

In Figures 8 and 9, a digital potentiometer is used to change the offset errors of a simple amplifier circuit.

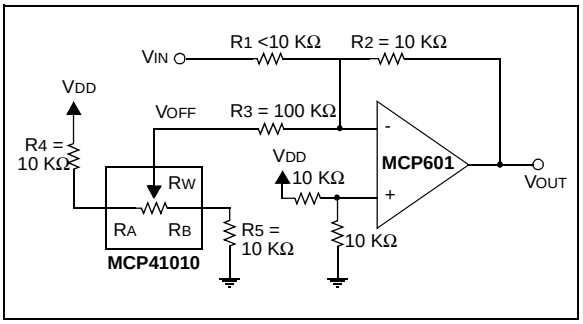


FIGURE 8: *A high resolution offset adjust circuit is implemented in this standard inverting amplifier configuration with the addition of a digital potentiometer, R_3, R_4 and R_5.*

In this circuit, the amplifier is configured in a inverting configuration. The transfer function for the input signal, V_{IN} is equal to:

$$V_{OUT} = -V_{IN}\left(\frac{R_2}{R_1}\right) + \frac{V_{DD}}{2}$$

An offset voltage is injected with the same voltage divider that was used in the circuit in Figure 5.b. The transfer function of the offset voltage, V_{OFF} is:

$$V_{OUT} = -V_{OFF}\left(\frac{R_2}{R_3}\right)$$

With the resistor values shown in the figure, the gain on the V_{IN} is 10V/V and the gain on V_{OFF} is 0.1V/V. With V_{DD} = 5V, the LSB size of the offset adjust circuitry is 651 µV.

With this configuration, the nominal errors and over temperature errors that are generated by the digital potentiometer is 10X smaller than the errors discussed in Figure 5.b.

Another method of implementing an analog offset adjustment with a digital potentiometer is shown in Figure 9.

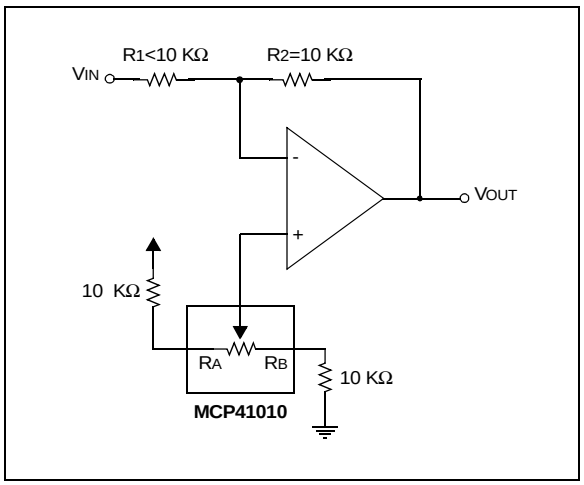


FIGURE 9: *A lower resolution offset adjust circuit using a digital potentiometer can be used to adjust large system offsets.*

In this circuit, the gain of the signal is equal to:

$$V_{OUT} = -V_{IN}\left(\frac{R_2}{R_1}\right)$$

And the gain of the offset adjust circuitry is equal to:

$$V_{OUT} = V_{DD}R_{POT-B}\frac{\left(1+\frac{R_2}{R_1}\right)}{(R_{POT-AB}+R_2+R_3)}$$

The offset adjustment circuit used in this application has the same topology as the circuit in Figure 5.b. Consequently, the errors due to this configuration is consistent with previous discussions.

Gain Adjust Amplifier Circuits

Circuit gain errors can compromise the analog dynamic range of a circuit. These types of errors can be easily calibrated out of the system digitally with the microcontroller, however, the analog dynamic range is never fully utilized. Consequently, analog gain adjustments are done where the full dynamic analog range is needed.

An example of an amplifier circuit that has an adjustable positive (noninverted) gain is shown in Figure 10.

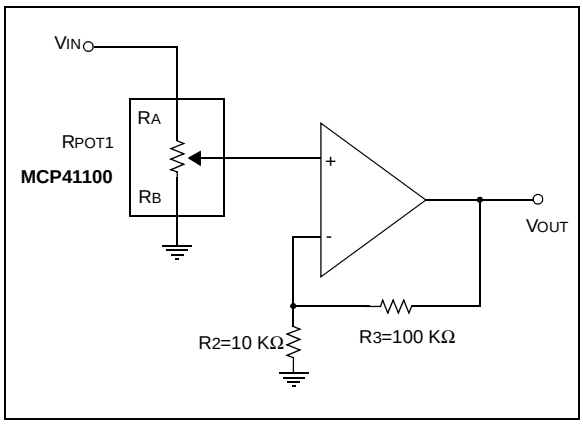


FIGURE 10: *An amplifier circuit designed with an adjustable noninverting gain.*

In this circuit, the transfer function is:

$$V_{OUT} = V_{IN}\frac{\left(1+\frac{R_3}{R_2}\right)}{\left(\frac{R_{POT1-B}}{R_{POT1-AB}}\right)}$$

The adjustable gain is implemented with the digital potentiometer, RPOT. Digital potentiometers that have higher nominal values are best suited for this circuit. Higher value resistances minimize the error that is contributed by the source resistance of VIN.

The maximum gain is equal to:

$$Gain\ (max) = \left(1+\frac{R_3}{R_2}\right)-\left(\frac{2^n-1}{2^n}\right)$$

Using the values of resistors in Figure 10:

$$\text{Gain (max)} = (1 + 100k\Omega/1k\Omega) - (2^8 - 1)/2^8$$
$$= 101.996V/V$$

At room temperature, the digital potentiometer's DNL error effects the circuit gain accuracy with gains that are lower 10% of the range (assuming DNL (max) = ±0.25 LSB). This relationship is shown graphically in Figure 11.

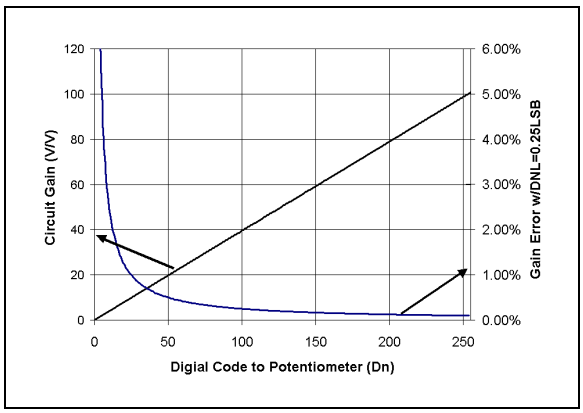


FIGURE 11: *For the circuit in Figure 10, the gain vs. digital code is linear. The maximum possible gain error is logarithmic, decreasing with higher digital potentiometer codes.*

In terms of temperature effects on the digital potentiometer in this configuration, the changes of R_A and R_B over temperature track at a rate of 800 ppm/°C (typ). Since these elements are configured as a mathematical ratio, this error is cancelled. The variance between the two elements over temperature is 1% (typ). This variance will be directly translated into gain error over temperature.

Another amplifier gain circuit that uses a digital potentiometer is shown in Figure 12. In this circuit, the amplifier circuit executes an inverting adjustable gain function.

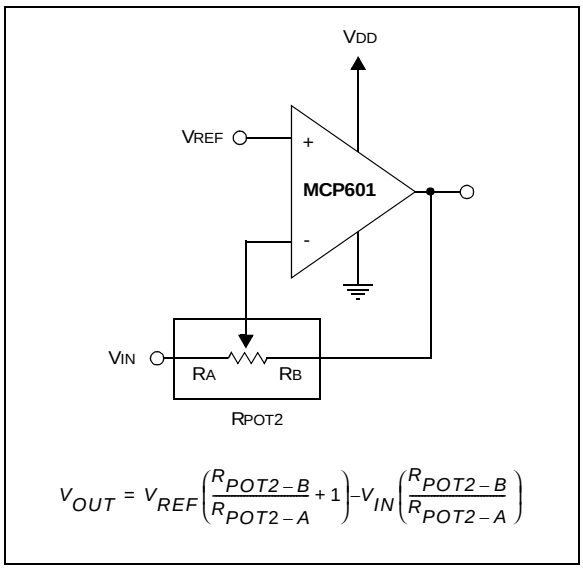


FIGURE 12: *This amplifier circuit uses a digital potentiometer to implement an adjustable inverting gain.*

The circuit transfer function is:

$$V_{OUT} = V_{IN}\left(\frac{R_{POT2-A}}{R_{4-B}}\right) + V_{REF}\left(\frac{R_{POT2-A}}{R_{POT2-B}}\right) + 1$$

With this circuit, the gain function versus digital potentiometer code is nonlinear as shown in Figure 13.

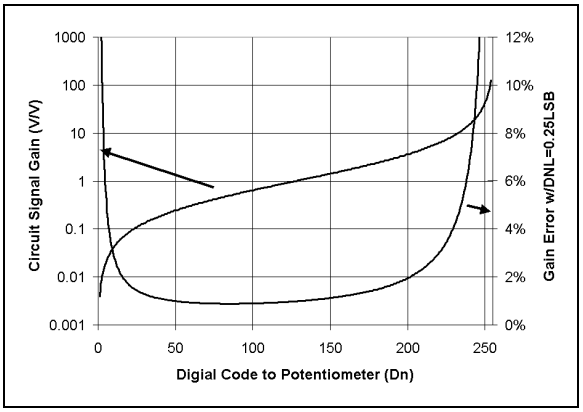


FIGURE 13: *The transfer function of V_{OUT} to V_{IN} of the circuit shown in Figure 12 has a nonlinear response over the code span of the digital potentiometer. This phenomena creates a circuit that gains the input signal below digital potentiometer codes of 128 and attenuates the signal with codes above 128.*

The nominal accuracy of this gain cell is minimized because the two sides of the digital potentiometer are ratioed in the circuit transfer function. Any gain error at room temperature is due to the DNL error of the digital potentiometer. The maximum effects of the error is shown graphically in Figure 13.

In terms of temperature effects on the digital potentiometer in this configuration, R_A and R_B are configured as a mathematical ratio in the transfer function. This cancels the change in the 800 ppm/°C (typ) resistive element. The variance between the two elements over temperature is 1% (typ). This variance will be directly translated into gain error over temperature.

The circuits in Figure 10 and Figure 12 can be combined to build an adjustable gain difference amplifier much like the circuit shown in Figure 3. This configuration is shown Figure 14.

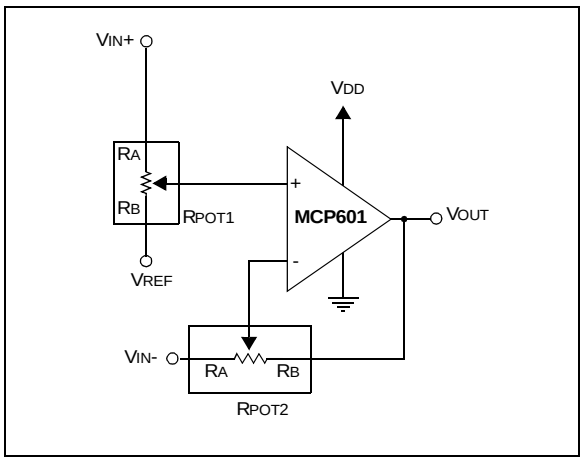


FIGURE 14: *A difference amplifier that has stable resistor matching and temperature coefficients.*

If the digital code setting for R_{POT1} and R_{POT2} are equal, the transfer function for this circuit is:

$$V_{OUT} = (V_1 - V_2)\left(\frac{R_{POTX-B}}{R_{X-A}}\right) + V_{REF}$$

The gain of this circuit ($V_{OUT}/(V_1-V_2)$) versus the digital potentiometer code is shown graphically in Figure 15.

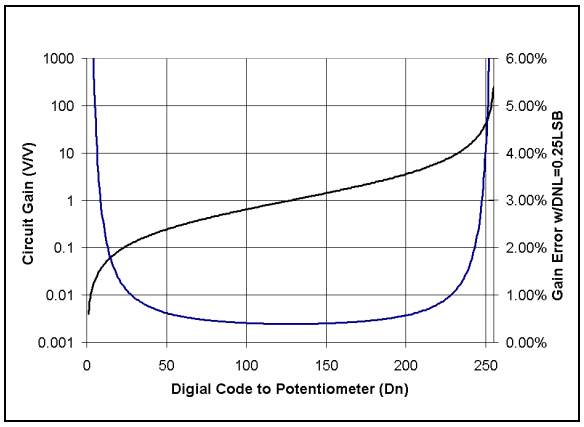


FIGURE 15: *The gain of circuit in Figure 14 is greater than one with digital code settings larger than 128 and between zero and one for digital code settings less than 128. The gain error, due to typical DNL errors, is less than 1% between 28 and 229.*

The temperature performance of this circuit is significantly improved over the circuit shown in Figure 3 because all of the resistors in this circuit are elements of the digital potentiometers.

Once again, the common-mode rejection (CMR) error that is attributed to resistor mismatches in this circuit is equal to:

$$CMR = 100\frac{\left(1 + \frac{R_1}{R_2}\right)}{\%\text{ of mismatch error}}$$

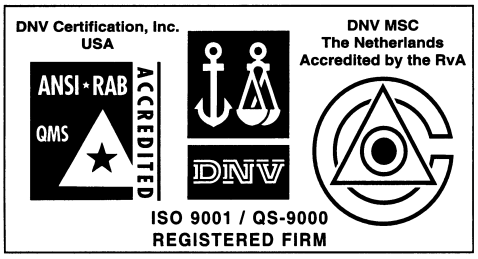
where (% of mismatch error) is the mismatch in the equation $R_1/R_2 = R_3/R_4$.

CONCLUSION

The digital potentiometer has entered the market with clear advantages over the mechanical potentiometer. Its programmability allows to change the offset, gain and voltage references reliably as well as on the fly. The effects of variances of the absolute resistances and temperature drifts can be minimized if good circuit design techniques are used.

NOTES:

Trademarks



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