

CD40106B Types

CMOS Hex Schmitt Triggers

High-Voltage Types (20-Volt Rating)

■ CD40106B consists of six Schmitt-trigger circuits. Each circuit functions as an inverter with Schmitt-trigger action on the input. The trigger switches at different points for positive- and negative-going signals. The difference between the positive-going voltage (VP) and the negative-going voltage (VN) is defined as hysteresis voltage (VH) (see Fig.6). The CD40106B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

Features:

- Schmitt-trigger action with no external components
- Hysteresis voltage (typ.) 0.9 V at VDD = 5 V, 2.3 V at VDD = 10 V, and 3.5 V at VDD = 15 V
- Noise immunity greater than 50%
- No limit on input rise and fall times
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Low VDD to VSS current during slow input ramp
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators

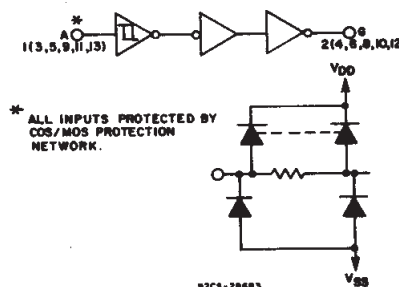
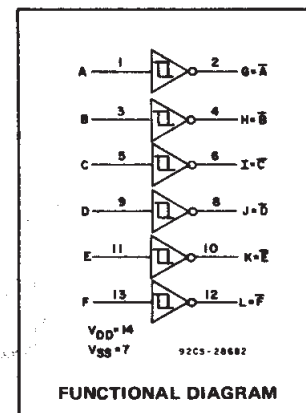


Fig.1 - Logic diagram (1 of 6 Schmitt triggers).

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (VDD)	-0.5V to +20V
Voltages referenced to VSS Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to VDD +0.5V
DC INPUT CURRENT, ANY ONE INPUT	±10mA
POWER DISSIPATION PER PACKAGE (PD):	
For TA = -55°C to +100°C	500mW
For TA = +100°C to +125°C	Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE (TA)	-55°C to +125°C
STORAGE TEMPERATURE RANGE (Tstg)	-65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For TA Full Package-Temperature Range)	3	18	V

DYNAMIC ELECTRICAL CHARACTERISTICS

At TA = 25°C, Input tr, tf = 20 ns, CL = 50 pF, RL = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		VDD (V)	TYP.		MAX.
Propagation Delay Time:	tPHL	5	140	280	ns
	tPLH	10	70	140	
		15	60	120	
Transition Time:	tTHL	5	100	200	ns
	tTLH	10	50	100	
		15	40	80	
Input Capacitance, CIN	Any Input		5	7.5	pF

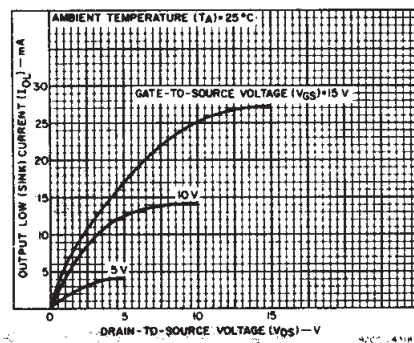


Fig.2 - Typical output low (sink) current characteristics.

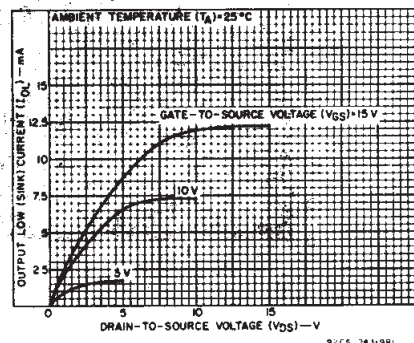
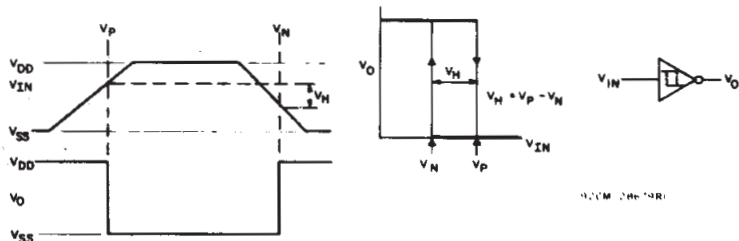


Fig.3 - Minimum output low (sink) current characteristics.

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	1	1	30	30	-	0,02	1	μA
	-	0,10	10	2	2	60	60	-	0,02	2	
	-	0,15	15	4	4	120	120	-	0,02	4	
	-	0,20	20	20	20	600	600	-	0,04	20	
Positive Trigger Threshold Voltage V _P Min.	-	-	5	2,2	2,2	2,2	2,2	2,2	2,9	-	V
	-	-	10	4,6	4,6	4,6	4,6	4,6	5,9	-	
	-	-	15	6,8	6,8	6,8	6,8	6,8	8,8	-	
	-	-	5	3,6	3,6	3,6	3,6	-	2,9	3,6	
	-	-	10	7,1	7,1	7,1	7,1	-	5,9	7,1	
	-	-	15	10,8	10,8	10,8	10,8	-	8,8	10,8	
Negative Trigger Threshold Voltage V _N Min.	-	-	5	0,9	0,9	0,9	0,9	0,9	1,9	-	V
	-	-	10	2,5	2,5	2,5	2,5	2,5	3,9	-	
	-	-	15	4	4	4	4	4	5,8	-	
	-	-	5	2,8	2,8	2,8	2,8	-	1,9	2,8	
	-	-	10	5,2	5,2	5,2	5,2	-	3,9	5,2	
	-	-	15	7,4	7,4	7,4	7,4	-	5,8	7,4	
Hysteresis Voltage V _H Min.	-	-	5	0,3	0,3	0,3	0,3	0,3	0,9	-	V
	-	-	10	1,2	1,2	1,2	1,2	1,2	2,3	-	
	-	-	15	1,6	1,6	1,6	1,6	1,6	3,5	-	
	-	-	5	1,6	1,6	1,6	1,6	-	0,9	1,6	
	-	-	10	3,4	3,4	3,4	3,4	-	2,3	3,4	
	-	-	15	5	5	5	5	-	3,5	5	
Output Low (Sink) Current, I _{OL} Min.	0,4	0,5	5	0,64	0,61	0,42	0,36	0,51	1	-	mA
	0,5	0,10	10	1,6	1,5	1,1	0,9	1,3	2,6	-	
	1,5	0,15	15	4,2	4	2,8	2,4	3,4	6,8	-	
Output High (Source) Current, I _{OH} Min.	4,6	0,5	5	-0,64	-0,61	-0,42	-0,36	-0,51	-1	-	mA
	2,5	0,5	5	-2	-1,8	-1,3	-1,15	-1,6	-3,2	-	
	9,5	0,10	10	-1,6	-1,5	-1,1	-0,9	-1,3	-2,6	-	
	13,5	0,15	15	-4,2	-4	-2,8	-2,4	-3,4	-6,8	-	
Output Voltage Low-Level, V _{OL} Max.	-	5	5			0,05			0	0,05	V
	-	10	10			0,05			0	0,05	
	-	15	15			0,05			0	0,05	
Output Voltage High Level, V _{OH} Min.	-	0	5			4,95		4,95	5	-	V
	-	0	10			9,95		9,95	10	-	
	-	0	15			14,95		14,95	15	-	
Input Current, I _{IN} Max.	-	0,18	18	±0,1	±0,1	±1	±1	-	±10 ⁻⁵	±0,1	μA



a) Definition of V_P, V_N, V_H
b) Transfer characteristics of 1 of 6 gates
Fig. 6 - Hysteresis definition, characteristics, and test set-up.

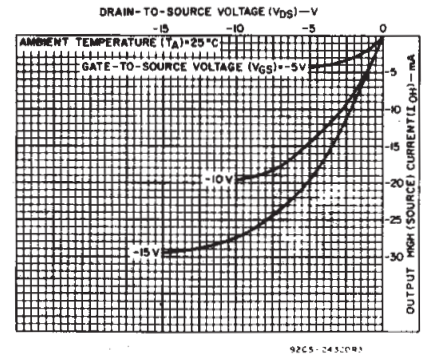


Fig. 4 - Typical output high (source) current characteristics.

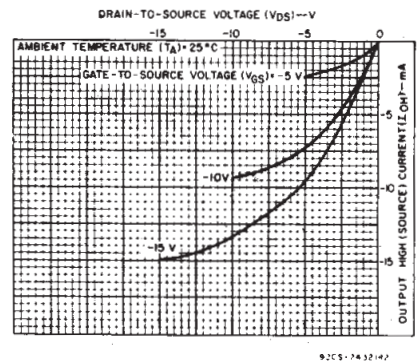


Fig. 5 - Minimum output high (source) current characteristics.

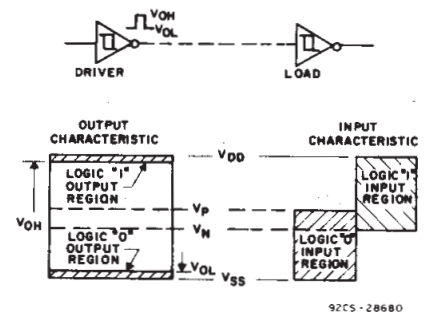


Fig. 7 - Input and output characteristics.

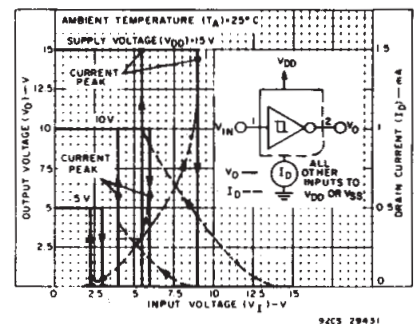


Fig. 8 - Typical current and voltage transfer characteristics.

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Fig. 9 - Typical voltage transfer characteristics as a function of temperature.

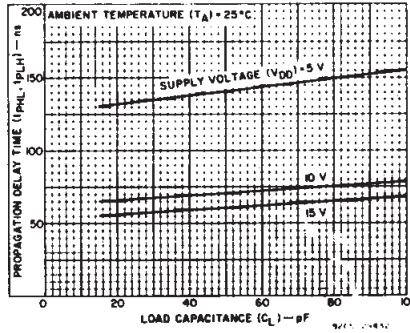


Fig. 10 - Typical propagation delay time as a function of load capacitance.



Fig. 11 - Typical transition time as a function of load capacitance.



Fig. 12 - Typical power dissipation per trigger as a function of input frequency.



Fig. 13 - Typical trigger threshold voltage as a function of supply voltage.

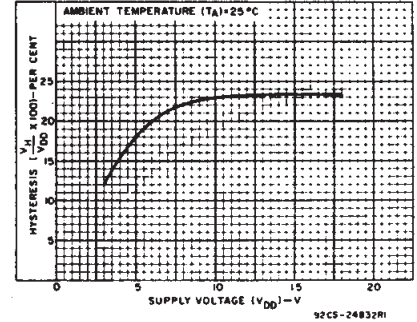


Fig. 14 - Typical per cent hysteresis as a function of supply voltage.

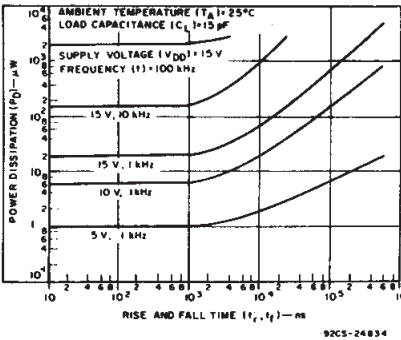


Fig. 15 - Typical power dissipation as a function of rise and fall times.

APPLICATIONS



Fig. 16 - Wave shaper.

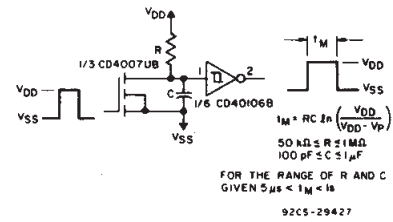


Fig. 17 - Monostable multivibrator.

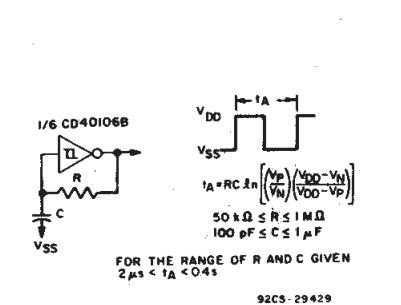


Fig. 18 - Astable multivibrator.

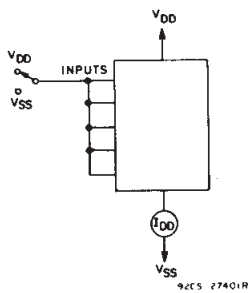


Fig. 19 - Quiescent device current test circuit.

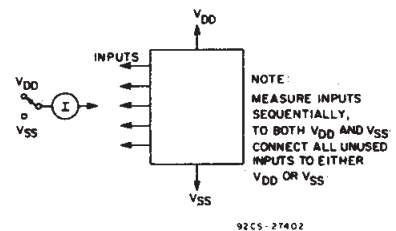


Fig. 20 - Input current test circuit.

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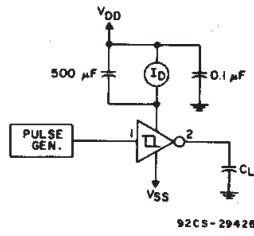
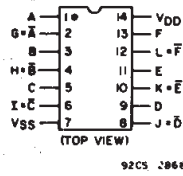
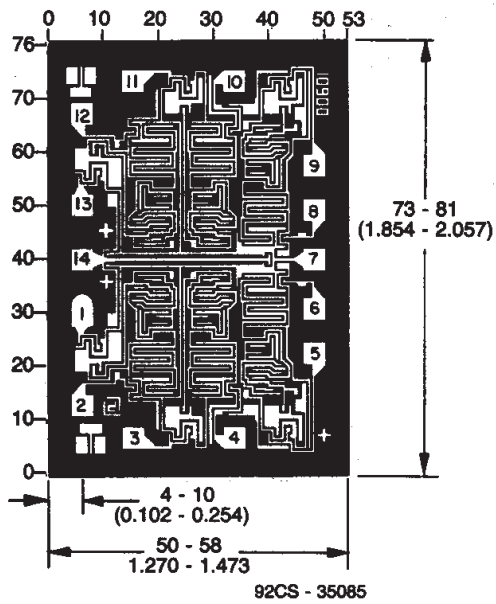


Fig.21 – Dynamic power dissipation test circuit.



TERMINAL ASSIGNMENT



Dimensions and Pad Layout for CD40106BH

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